Ph.D. DISSERTATION

WSe_2 Field Effect Transistor Fabrication and Characterization

WSe_2를 사용한 전계 효과 트랜지스터의 제작과 특성 분석

BY

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2016 년 2 월

서울대학교 대학원

전기정보공학부

조 인 탁

조인탁의 공학박사 학위논문을 인준함

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ABSTRACT

Recently, transition metal dichalcogenides (TMDCs) have been investigated as candidate materials for next generation nano electronic devices with their outstanding electrical, optical and thermo-mechanical properties. Among various TMDCs FET, especially WSe_2 FET, has drawn attention to the possibility for its applications of nanoscale complementary circuits and switching back planes for high resolution flat panel display (FPD) due to their high mobility (~100 $cm^2/V \cdot s$), excellent on/off ratio (~10^7), and low subthreshold slope (*SS*, ~ 70 mV/decade).

In this thesis, high performance TMDC field effect transistors (FETs) were fabricated by mechanically exfoliated multi-layer WSe_2. In the DC measurement result, large hysteresis is observed due to the gate bias stress during the measurement. However, in the Pulsed *I-V* measurement, negligible hysteresis gap and enhanced conductance are obtained with an optimized measurement condition (V_{base} = 0 V, t_{on} = 10^{-4} s and t_{off} = 1 s). Adopting the hydrogen annealing and hydrophobic CYTOP encapsulation layer, the device performance has improved dramatically.

From the low frequency noise measurement result, fabricated multilayer WSe_2 FET obey consistently Hooge's empirical relation, which indicates mobility fluctuation is a dominant mechanism responsible for the drain current

fluctuation. Although low frequency noise measure at different temperature, the mechanism of low frequency noise is not changed. However, Hooge`s parameter slightly increased with temperature increase due to phonon scattering enhancement. These results are explained with the help of model incorporating Thomas-Fermi charge screening and inter-layer resistance coupling.

High performance complementary metal oxide semiconductor (CMOS) logic inverter was implemented by fabricating p-and n-type field effect transistors (FETs). Both the p-type FET with a high work-function metal and the n-type FET with a low work-function metal show similar on-current densities ($>10^6$A) and on/off current ratios ($>10^4$). The proposed inverter shows excellent switching characteristics including relatively high voltage gains and high noise margins. This work has great significance in terms of realization of CMOS logic device based on TMDCs without additional doping scheme.

Lastly, contact property improve using an oxygen plasma treatment method. After plasma treatment, WO_3 was formed at WSe_2 flake surface. WO_3 plays a role as hole injection layer between Ni and WSe_2 flake. Contact resistance and undesirable Schottky barrier height reduced dramatically. This has the advantage of being easy to process and method do not need an additional deposition process.

Keywords: TMDC, WSe_2, field effect transistor, pulsed-IV, low frequency noise

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CONTENTS

Chapter 1

Introduction

1. 1 Motivation

A thin film transistor (TFT) is a distinctive type of field effect transistor (FET) formed by depositing thin films of the dielectric layer as well as an active semiconductor layer and metallic contacts onto a substrate [1]. In 1962, first operative TFT was reported by P. K. Weimer [2]. Since the Spear and LeComber reported on the doping capability of hydrogenated amorphous Silicon (a-Si) by the glow discharge technique and demonstrated of functional a-Si TFT, whose structure and transfer characteristics are shown in Fig 1.1, for the first time in the later of 1970's [3]. Among the various TFTs, Si based TFTs have successfully influenced the large area liquid crystal displays (LCD) technology and become the most important devices for active matrix liquid crystal and organic light emitting diode applications (OLED) [4]. However, because of the, the low mobility (<1 cm^2/Vs) and threshold voltage instabilities, a-Si TFTs have reached the uppermost limits which have to be surmounted to implement high brightness and high definition displays. Also, low mobility characteristic of a-Si TFTs make it difficult to integrate peripheral circuits. In the case of polycrystalline

Silicon (poly-Si) TFTs, low temperature polycrystalline silicon (LTPS) TFTs are widely used for the pixel devices of AMOLED because of their high current-driving capability owing to high mobility (>100 cm^2/Vs). Nevertheless, the problems of high manufacturing cost exist. Moreover, the variations in the grain size and gate-oxide trap density in poly-Si bring the non-uniformity of their mobility and threshold voltage over large area [5]. For these reasons, high mobility and CMOS available TFT needs for high definition and large scale display back plane. Table 1-1 summarizes the properties of the available TFT technologies. In the Table 1-1, TMDC FETs demonstrate the potential for better device characteristics in terms of mobility, capability of CMOS implementation, and low cost as a merit. With the continuous research and development efforts, TMDC FET technology is believed to be an attractive alternative to existing TFT technologies soon.

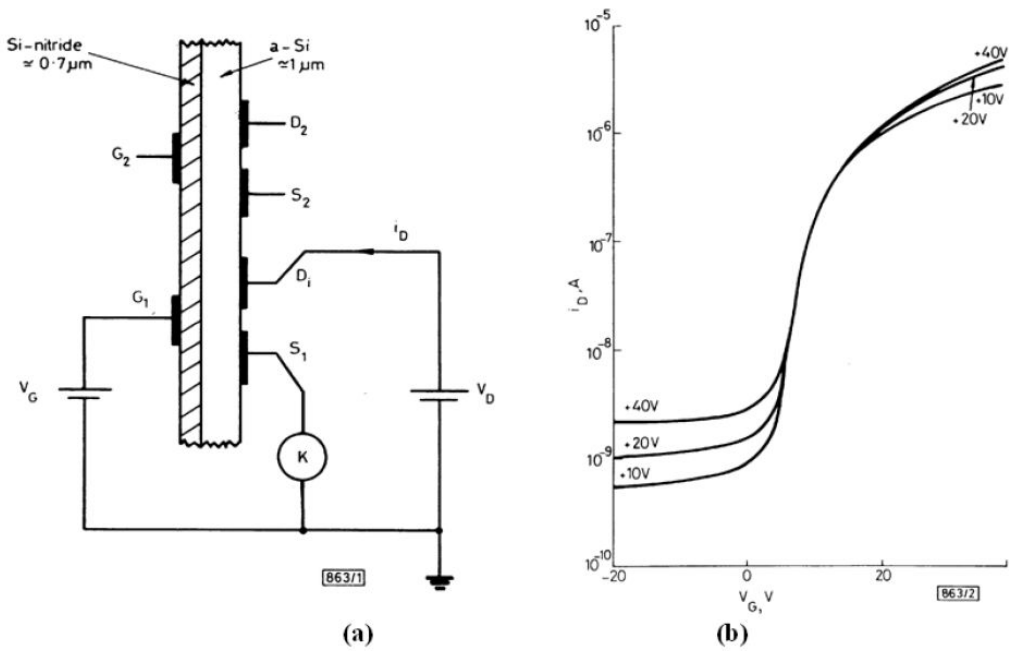


Fig. 1.1 First a-Si TFT (a) structure and (b) transfer curves.

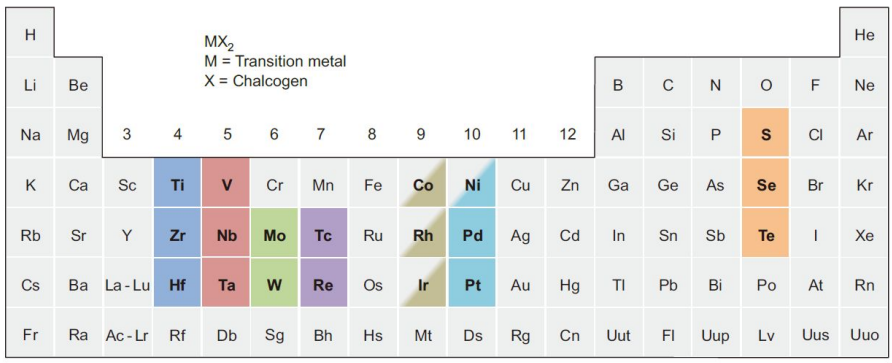
Table 1-1 Comparison of available TFT technologies.

	Poly-Si TFT	a-Si:H TFT	Organic TFT	Oxide TFT	TMDC FET
Type	CMOS	CMOS	CMOS	NMOS	CMOS
-Mobility	Good	Poor	Poor	Good	Good
-Leakage Current	Medium	Low	Medium	Low	Medium
-Uniformity	Poor	Good	Good	Good	NA
Cost	High	Low	Very low	Medium	Low
Processing Temperature	High	Low	Very low	Very low	High

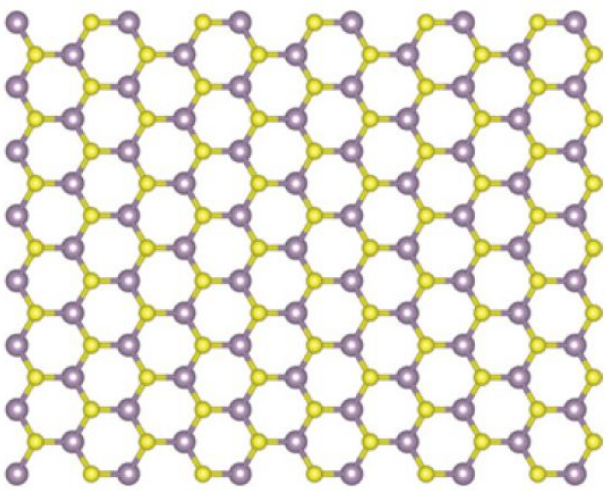
1. 2 TMDC

Recently, ultra-thin films of transition metal dichalcogenides (TMDCs) [6] have been actively studied for the alternative opportunities to serve as two dimensional (2D) active layers beyond graphene. Particularly, TMDCs, which have intrinsic band gaps [7, 8], are very attractive for the envisioned nano-electronic applications due to its unique electrical [9, 10], chemical [11, 12], and optical properties [13]. The TMDC is composed to chemical formula MX_2, where M stands for a transition metal and X for Se, S, or Te. Single crystals of TMDC are formed by stacks of X–M–X layers [14]. In Fig 1. 2 and 3 [1, 14], group 4–7 TMDs are predominantly layered, whereas some of group 8–10 TMDs are commonly found in non-layered structures [14]. In layered structures, each layer typically has a thickness of 6~7 Å, which consists of a hexagonally packed layer of metal atoms sandwiched between two layers of chalcogen atoms. In single layer TMDC, each atoms are held together by covalent bonds, whereas the layers are weakly bonded to each other by van der Waals forces [14]. For this reasons, many research group study about single and bilayer TMDC FET. Furthermore, multilayer TMDC FET research was also widely studied as optical device and TFT application for large scale display pannel due to their high mobility (> 100 cm^2/Vs), excellent on/off ratio (~10^7) and low subthreshold swing(SS, ~70 mV/dec.) [15, 16]. Among various TMDC layers, predominant

research activities have been noticeably toward single or/and multi-layer MoS_2 field effect transistors (FETs) with typical n-type characteristics associated with relatively easy preparation of thin films via exfoliation or/and chemical vapor deposition (CVD) [17], compared with other candidates in TMDCs. However, WSe_2 FETs with typical p-type properties can be very appealing for the applications of nanoscale complementary circuits and switching backplanes for flat panel display (FPD) [15, 16].



(a)



(b)

Fig. 1.2 (a) The transition metals and the three chalcogen elements that predominantly crystallize in those layered structure are highlighted in the periodic table. Partial highlights for Co, Rh, Ir and Ni indicate that only some of the dichalcogenides form layered structures. For example, NiS_2 is found to have apyrite structure but $NiTe_2$ is a layered compound. (b) c-Axis and section view of single-layer TMD [14].

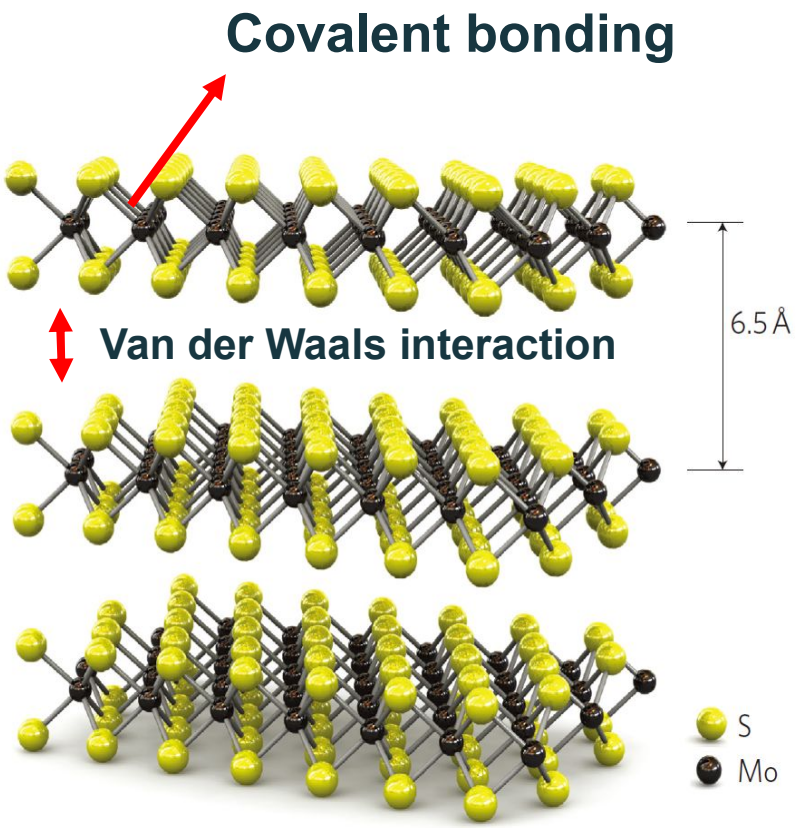


Fig. 1.3 The atomic structure of MoS_2 [6].

1. 3 Thesis Organization

This thesis is organized as follows. Chapter 1 provides motivation of this thesis including an overview of TMDC FET. Chapter 2 consists of a fabrication process of mechanically exfoliated multi-layer WSe_2 FET, and their current-voltage (*I-V*) characteristics. Chapter 3 is a measurement result of pulsed *I-V* and DC *I-V* of fabricated WSe_2 FET. Through the pulsed *I-V* and DC *I-V*, negligible

hysteresis gap and enhanced conductance are obtained with an optimized measurement condition. Chapter 4 show the low frequency noise characteristic of WSe_2 FET. Chapter 5 represents n/p-channel WSe_2 FET fabrication and CMOS inverter implementation. Chapter 6 represents contact property improvement method. Chapter 7 is conclusion of this thesis.

.

Chapter 2

WSe_2 FET fabrication

2. 1 Fabrication Process

- ***Substrate preparation (heavily doped Si –gate, SiO_2–gate insulator)***
- ***ID mark (lift-off process - Cr)***
- ***TMDC flake transfer (PDMS stamp)***
- ***Annealing (350 ^oC, 2 hours, H_2 : Ar = 1 : 1)***
- ***Source/Drain formation (lift-off process)***
- ***Flake thickness measurement (AFM)***
- ***Passivation – Hydrophobic CYTOP***
- ***Pad open - RIE etch (CF_4, SF_6)***
- ***Measurement (Agilent B1500)***

Fig. 2.1 Fabrication process flow of WSe_2 FET

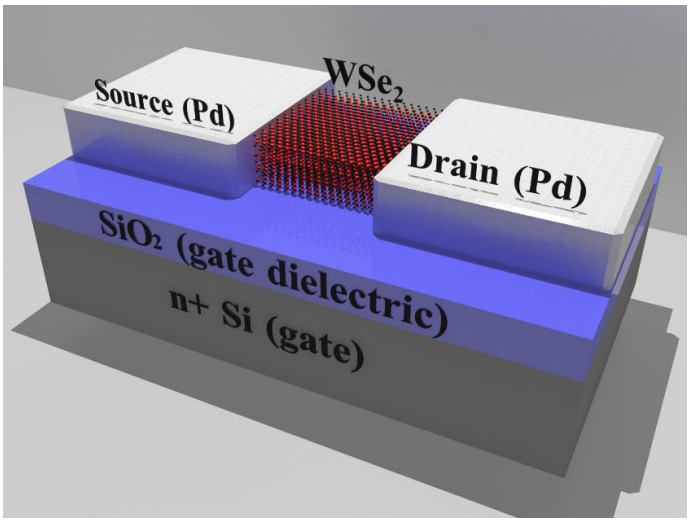


Fig. 2.2 Schematic image of a multilayer WSe_2 FET.

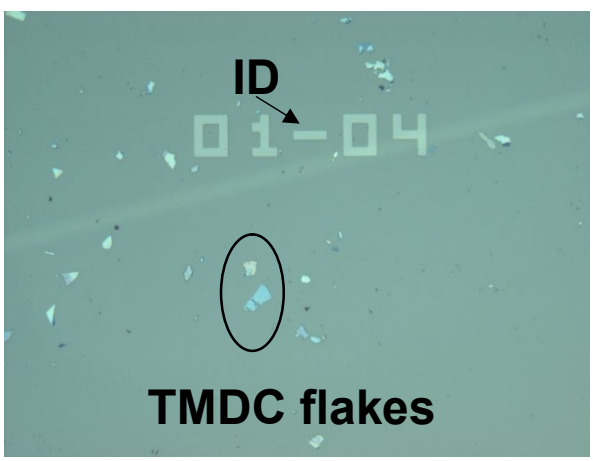


Fig. 2.3 Align mark and WSe_2 flakes transferred onto the SiO_2/Si substrate by using PDMS stamps.

Fig. 2.1 and 2 show fabrication process flow of WSe_2 FET and the perspective view of a multilayer WSe_2 FET with a bottom gate structure. An n-type silicon wafer with heavy phosphorus doping (ρ~0.005 ohm/cm) was used as a starting substrate which also play a role as back gate electrodes. After thermal oxidation in dry oxygen at 950°C, 10 nm thick thermal oxide was grown on the heavily doped Si wafer and serves as gate insulator. Fig. 2.3 show the align mark and WSe_2 flakes transferred onto the SiO_2/Si substrate. Photoresist (PR) patterning for lift off and Cr deposition (~50 nm) are followed by PR removal to form alignment marks on each sample. WSe_2 flakes were mechanically exfoliated from bulk WSe_2 crystals by using PDMS stamps and immediately transferred onto the SiO_2/Si substrate. The multi-layer WSe_2 flakes on the substrate were annealed at 350 ºC for 2 hours in the ambient of a mixed gas of argon and hydrogen. Photolithographic pattering and electron-beam evaporation of Pd (~50 nm), followed by lift-off in acetone, creates source and drain electrodes on WSe_2 with good Ohmic contact [11]. Fig 2.4 shows the *I-V* characteristic of Pd-WSe_2-Pd vertical structure. In Fig 2.4, Ohmic behavior was clearly shown. After forming

S/D electrodes on WSe_2 flakes, layer thickness for each device was measured by atomic force microscopy (AFM). Finally, the backside of the WSe_2 flake was encapsulated by fluorinated polymer (CYTOP; CTL-809M, Asahi Glass Co., Ltd) with typical spin coating process. After thermal evaporation of SiO_X(~50 nm) on the CYTOP, for a surface promoter layer during PR coating, pad opening was completed by dry etching (~SF_6/CF_4) via PR patterns.

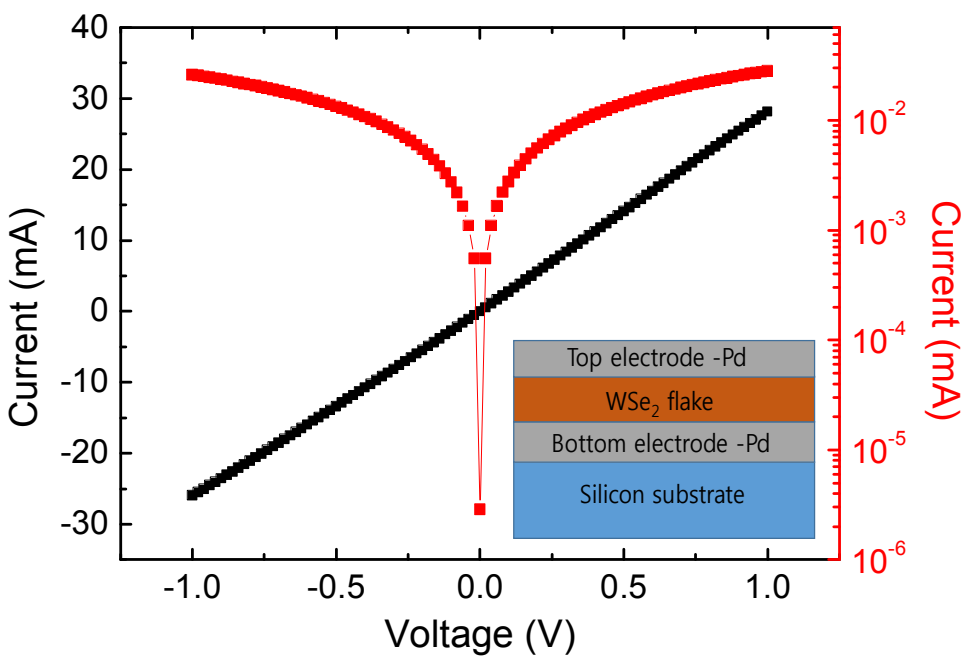


Fig. 2.4 *I-V* characteristic of Pd-WSe_2-Pd vertical structure.

2. 2 *I-V* characteristics with or without hydrogen annealing and passivation

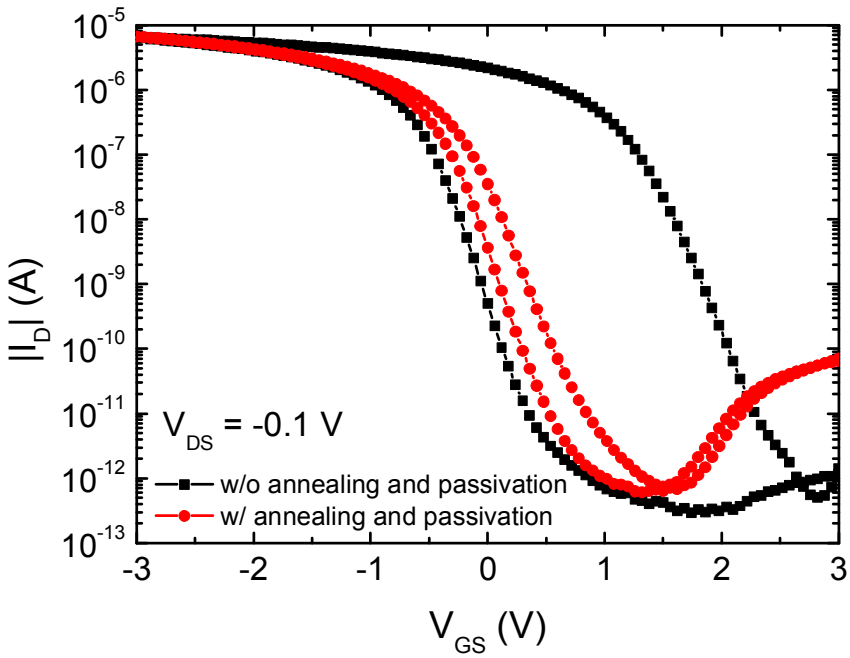
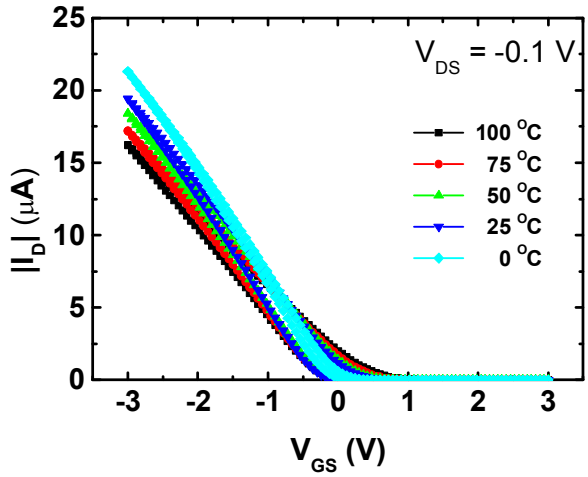


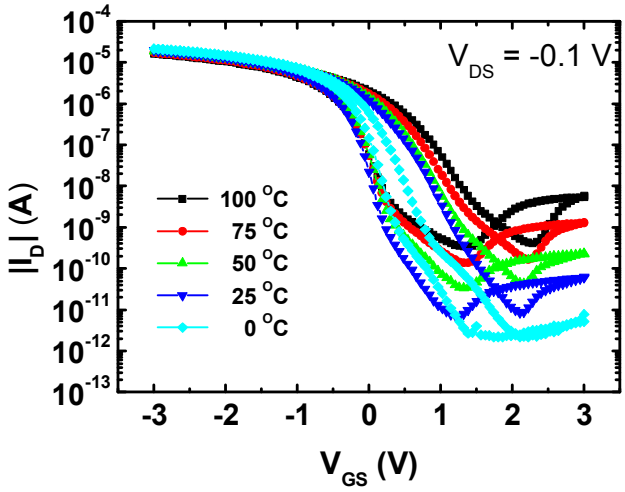
Fig. 2.5 Transfer characteristics for multilayer WSe_2 FETs with or without hydrogen annealing and CYTOP passivation measured in the linear operation regime at the drain bias of V_{DS}= -0.1V.

Fig. 2.5 shows the transfer characteristics of a fabricated multilayer WSe_2 FET with a ratio of width to length (W/L=30/10 μm) at a drain-to-source voltage (V_{DS}) of -0.1 V. The electrical characteristics of the devices were measured by using a precision semiconductor parameter analyzer (Agilent B1500A). In Fig 2. 2, the multilayer WSe_2 FETs with hydrogen annealing and CYTOP passivation show a negligible hysteresis gap (ΔV_{HYS} = ~0.5 V), indicating that hydrogen annealing process leads to the elimination of possible candidates of traps on the surface of the multilayers of WSe_2 associated with adsorbates (i.e., moisture or/and carbon residues) [18, 19].

2. 3 Temperature effect on *IV* characteristics



(a)



(b)

Fig. 2.6 (a) Linear and (b) log scale transfer curves of multilayer WSe_2 FET measured at various temperature (0 ~ 100 °C)

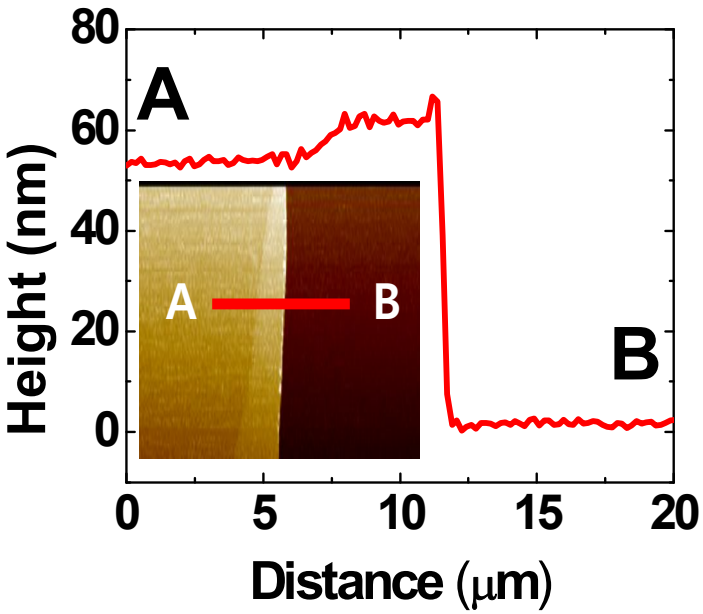


Fig. 2.7 Height profile for a multilayer in the channel of representative WSe_2 FETs. The inset shows the AFM images for the channel regime for WSe_2 FETs

Fig. 2.7 depicts height profile at the edge of the flake. The inset was AFM image of a fabricated multilayer WSe_2 FET. From AFM measurements, the thickness of the active layer used for measurement was 50 nm in chapter 2.3.

Fig 2. 6 show the transfer curves measured at various temperatures with a ratio of width to length (W/L=30 /10 μm) at a drain-to-source voltage (V_{DS}) of -0.1 V. In the all temperature range (0 ~ 100 ^{o}C) of measurement, the curves show typically observed p-type behaviors. In the Fig. 2.6 (b), *SS.* degradation was

observed between 10^{-8} A and 10^{-12} A. It is because of thickness effect of active layer. In the inset of Fig 2. 7, the thickness of the active layer on the same channel represents the difference of 10nm between point A and B. It means that effective gate bias of thick-active region for channel depletion is higher than thin-active region.

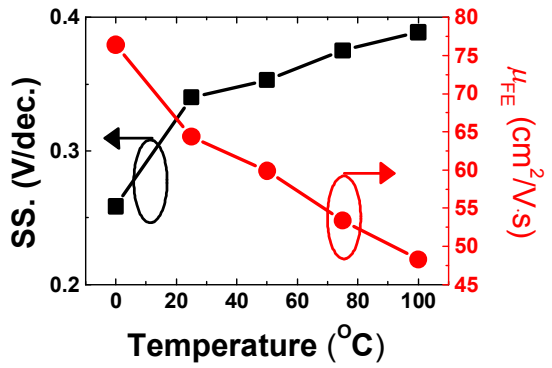
Fig. 2.8 show temperature dependency on electrical parameters extracted from transfer curves of multilayer WSe_2 FETs. The field effect mobility was extracted from maximum point of transconductance (g_m).

$$\mu_{eff} = \frac{Lg_m}{WC_iV_{DS}} \qquad \text{Eq. (2.1)}$$

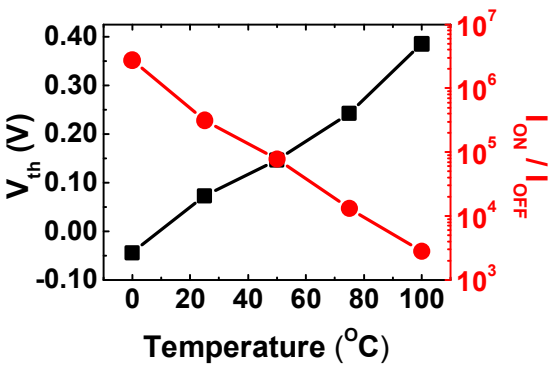
Where C_i and g_m are the gate capacitance per unit area and the transconductance, respectively. The current on/off ratio was defined as I_{on} ($|I_D|$ at V_{GS} = -3 V) / I_{off} ($|I_D|$ at V_{GS} = 3 V). The *SS.* was defined as V_{GS1} (V_{GS} at $|I_D| = 10^{-8}$ A) – V_{GS2} (V_{GS} at $|I_D| = 10^{-7}$ A). The threshold voltage (V_{th}) was calculated by fitting a straight line to the measured transfer curve. The hysteresis was defined as $V_{GS\_forward\ sweep}$ (at $|I_D| = 10^{-7}$ A) - $V_{GS\_reverse\ sweep}$ (at $|I_D| = 10^{-7}$ A). The μ_{eff} and

current on/off ratio were deteriorated as the temperature increases from 0°C to 100°C. Considering that phonon scattering is enhanced with increasing temperature, and leads to the degradation in the mobility [16]. Furthermore, the off-current increased with temperature increase and threshold voltage shift the positive direction, due to the increase of thermally activated carrier density. The SS, and hysteresis increased with temperature increase. In the MOSFET theory, the SS value is proportional to temperature.

$$SS. \propto KT / q \qquad \text{Eq. (2.2)}$$



(a)



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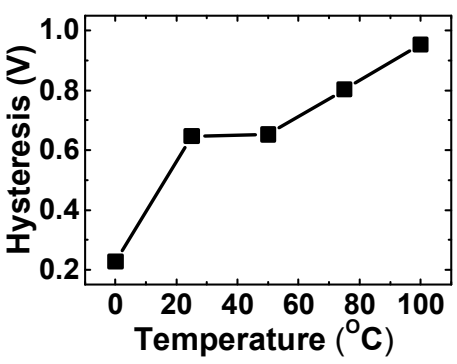


(c)

Fig. 2.8 Temperature dependency of (a)subthreshold slope, filed effect mobility, (b)threshold voltage, current on/off ratio and (c) hysteresis. All parameters extracted from transfer curves.

Chapter 3

DC, Fast and Pulsed *I-V* measurement for WSe_2 FET

3. 1 Introduction

Pulsed current-voltage (*I-V*) measurement is becoming an invaluable method for evaluating the performance and reliability of semiconductor devices. The goal of pulsed *I-V* measurement is to avoid the negative effects of self-heating and transient trapped charges, which can result in misleading test results. And pulsed *I-V* testing provides the accurate device data needed for improved computeraided-engineering (CAE) software models. In the case of TMDC FETs without hydrogen annealing and passivation, large hysteresis gap is observed under both air and vacuum environments, [20] which may cause uncertainty in the device characterization once any sweeping rate/range/direction of the gate/drain biases and/or the previous measurement state. The origin of their hysteretic and transient behaviors is largely due to absorption of moisture on the surface and intensified

by high photosensitivity of TMDCs. On the other hand, the hysteretic behaviors are typically attributed to charge trapping into the dielectric substrate. To reduce the hysteresis, the pulsed *I–V* measurement technique has been introduced to carbon nanotube (CNT) [21], graphene FETs [22, 23] and a few TMDCs FETs [24], however, in WSe_2 FETs, the effect of various parameters such as width time (t_{width}) in the fast *I-V*, turn-on and turn-off times (t_{on} and t_{off}) and V_G during t_{off} (V_{base}), in the pulsed *I-V* measurement have not been systematically reported yet. In this chapter, the *I-V* characteristics in WSe_2 FETs with the direct current (DC), fast *I-V*, and pulsed *I-V* methods have been investigated.

3. 2 Measurement set-up

The fast *I-V* and pulsed *I-V* measurements are carried out by using a Waveform Generator and Fast Measurement Unit (WGFMU) measurement system based on an Agilent B1500 semiconductor parameter analyzer for investigating the *I-V* characteristics of WSe_2 FETs. Fig. 3.1 show the scheme of pulsed *I-V* and fast *I-V*. In the fast *I-V* measurement, a width time (t_{width}) of the V_G pulse is modulated to change V_G sweeping rate. The t_{on} and t_{off} of the V_G pulse are changed in the pulsed *I-V* measurement. The V_G during t_{off} is set to 0 V, and the drain bias (V_D) is set to -0.1 V and 0 V. All measurements are performed under air ambient conditions at room temperature using double sweep method to see the hysteretic behavior clearly.

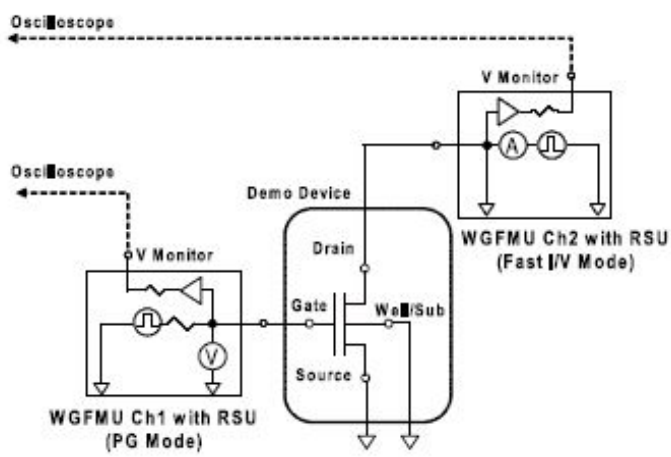


Fig. 3.1 Scheme of pulsed *I-V* and fast *I-V*.

3. 3 Measurement results

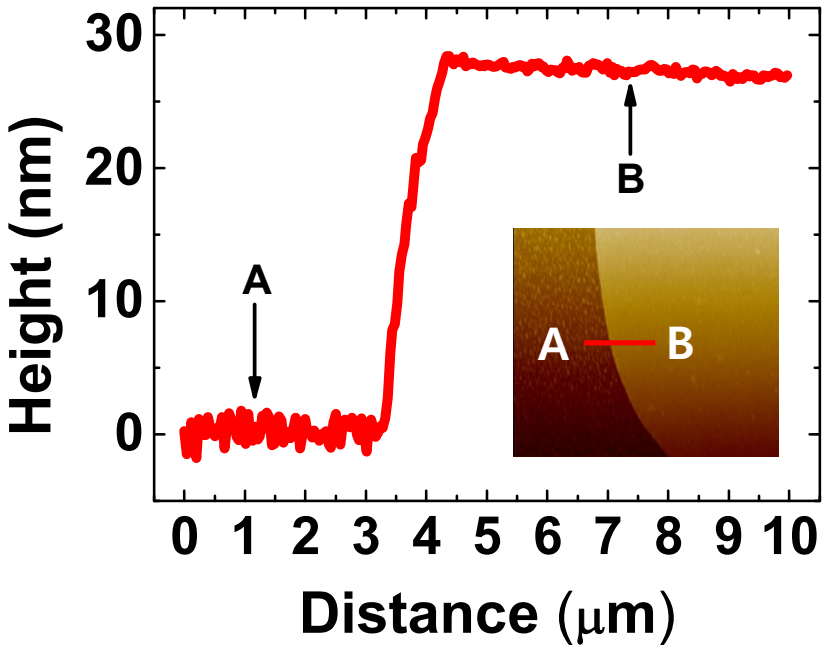


Fig. 3.2 Height profile for a multilayer in the channel of representative WSe_2 FETs. The inset shows the AFM images for the channel regime for WSe_2 FETs

In this chapter, the device used for measurement was not hydrogen annealed and passivation process for observation clear hysteresis gap. Fig. 3.2 depicts height profile at the edge of the flake. The inset was AFM image of a fabricated multilayer WSe_2 FET. From AFM measurements, the thickness of the active layer used for measurement was about 30 nm in chapter 3.3.

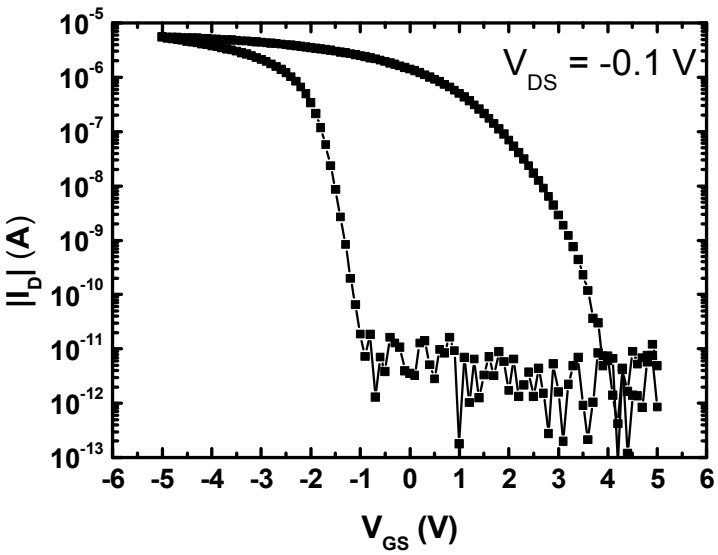


Fig. 3.3 I_D-V_{GS} characteristics of WSe_2 FET measured by using a dc method. Hysteretic behaviors are clearly observed.

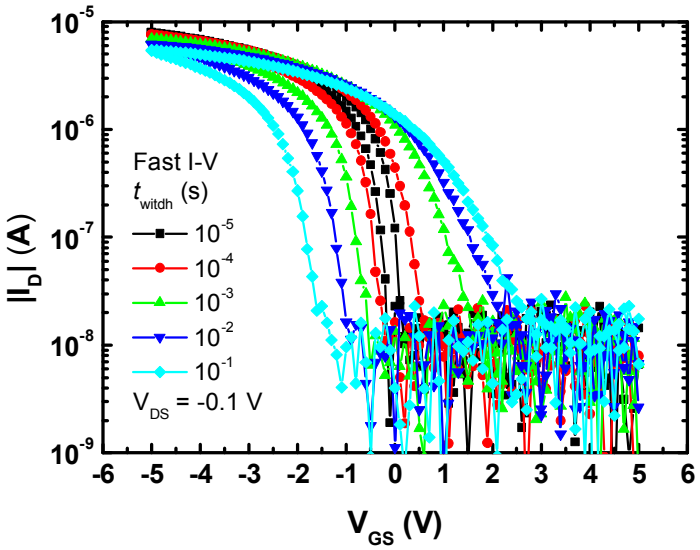


Fig. 3.4 I_D-V_{GS} characteristics of WSe_2 FET measured by FIV method as a parameter of t_{width}. As the V_G sweeping rate becomes faster with shorter t_{width}, less hysteresis and enhanced conductance are observed.

Fig. 3. 3 shows the I_D-V_{GS} characteristics measured by the DC method, and the hysteresis is clearly observed. Due to the V_G stress during the measurement, the charges are trapped or de-trapped at the WSe_2/SiO_2 interface and/or the backside of WSe_2 flakes, thus the threshold voltage (V_{th}) can be shifted to the right or left. In the result, the hysteresis (ΔV_{th}) occurs and the drain current decreases, which seems to be degradation of mobility and conductance. Since the charges remain trapped until the gate polarity is switched in the DC measurement [25], the large hysteresis is observed in a DC measurement.

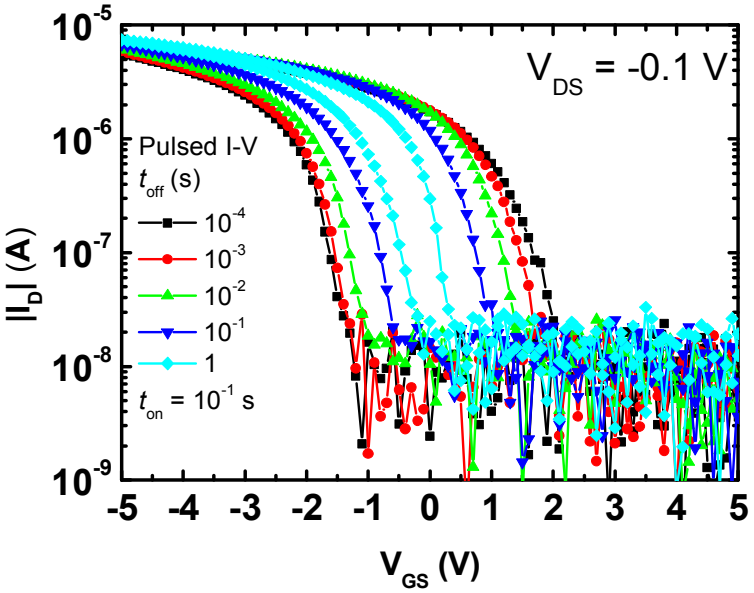
Fig. 3. 4 shows the I_D-V_{GS} curves measured by fast *I-V* method having a faster sweeping rate than that of the dc method as a parameter of t_{width}. Since faster sweeping rate reduces measuring time which results in less V_G stress during the measurement, the reduced hysteresis and enhanced mobility are achieved as t_{width} decreases. Although the results of fast *I-V* measurement with short t_{width} shows less hysteresis compared with that of dc measurement, the hysteresis is still not negligible even for the shortest t_{width} of 10^{-5} s. To reduce hysteretic behaviors of the I_D-V_G characteristics in WSe_2 FETs, the pulsed *I-V* measurement is a good

candidate, and the pulsed *I-V* method with various t_{on} and t_{off} should be systematically investigated.

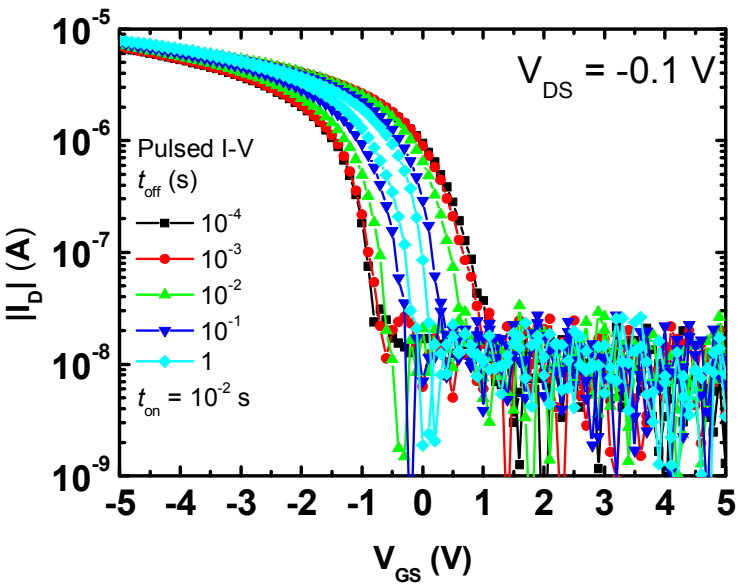
Fig. 3. 5 and 6 show the I_D-V_{GS} characteristics in WSe_2 FET measured by pulsed *I-V* method with the t_{off} varying from 10^{-4} s to 1 s at a t_{on} of 10^{-1} s, 10^{-2} s, 10^{-3} s and 10^{-4} s, respectively. The V_G pulse during t_{off} (V_{base}) is set to 0 V to minimize the V_G stress effect [23], and V_{DS} is -0.1 V. At a fixed t_{on}, less hysteresis and enhanced mobility and conductance are observed as t_{off} increases. The trapped charges by V_G stress during t_{on} can be detrapped during t_{off}, which helps the WSe_2 FETs to have a stress-free state, thus the hysteretic behavior is reduced as t_{off} increases. The t_{off} dependency is more apparent with longer t_{on}, then the t_{on} dependency of the I_D-V_{GS} curves are investigated. Fig. 3.7 shows the I_D-V_{GS} characteristics in WSe_2 FET measured by pulsed *I-V* method with the t_{on} varying from 10^{-1} s to 10^{-4} s at a t_{off} of 1 s. The V_{base} and V_{DS} are 0 V, and -0.1 V, respectively. At a fixed t_{off}, less hysteresis and enhanced mobility and conductance are observed as t_{on} decreases since shorter t_{on} gives less V_G stress during t_{on}. Particularly, we could obtain the intrinsic characteristics of WSe_2 showing

ignorable hysteresis and remarkably enhanced mobility (~160 cm/V·s) at a t_{on} of 10^{-4} s and a t_{off} of 1 s. Therefore, the pused *I-V* measurement with a short t_{on} for reducing charge trapping and a long t_{off} at a V_{base} of 0 V for increasing detrapping of trapped charges is the best way to obtain the intrinsic *I-V* characteristics in WSe_2 [23]. In Fig. 3.8, the I_D-V_{GS} curves measured by the DC, fast *I-V* (t_{width} of 10^{-5} s), and pulsed *I-V* (t_{on} of 10^{-4} s, t_{off} of 1 s, and V_{base} of 0 V) methods are compared. Among the I_D-V_G curves measured by the DC, fast *I-V*, and pulsed *I-V* methods, the pulsed *I-V* measurement method gives hysteresis-free I_D-V_{GS} curves with the best mobility. Fig. 3.9 shows I_D-V_{DS} characteristics in WSe_2 FET measured by pulsed *I-V* (t_{on} = 10^{-4} s, t_{off} = 1s, V_{base} = 0V). I_D-V_{DS} curves measured by pulsed *I-V* method are clearly saturated, whereas I_D-V_{DS} curves measured by DC method seem not saturated. Above mentioned, the V_G stress during the measurement, the charges are trapped or de-trapped at the WSe_2/SiO_2 interface and/or the backside of WSe_2 flakes, thus the threshold voltage (V_{th}) can be shifted to the right or left. In case of I_D-V_{DS} measurement, $|V_{GS}-V_{th}|$ is higher than 0 V. Therefore, V_{th} is shifted negative bias direction. However, V_{th} is shifted positive

bias direction with increasing V_{DS}. Fig. 3.10 shows I_D-V_{GS} characteristics in WSe_2 FET measured with various V_{DS} (-0.1, 0.5, and -1 V).

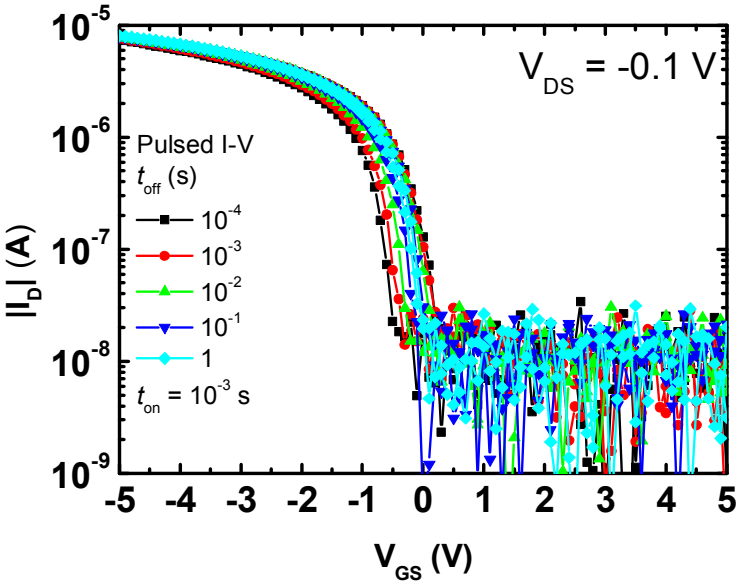


(a)

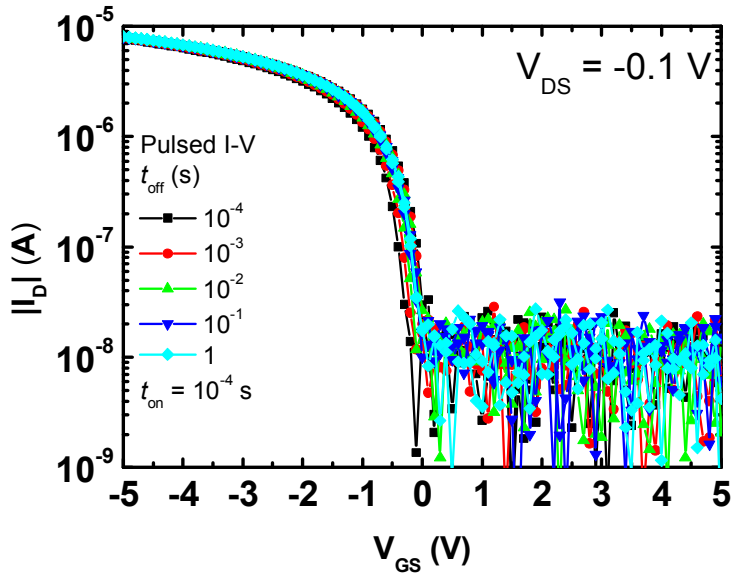


(b)

Fig. 3.5 I_D-V_{GS} characteristics in WSe_2 FET measured by pulsed *I-V* method with (a) the t_{off} varying from 10^{-4} s to 1 s at a t_{on} of 10^{-1} s, (b) the t_{off} varying from 10^{-4} s to 1 s at a t_{on} of 10^{-2} s. The V_{base} and V_D are 0 V, and -0.1 V, respectively.



(a)



(b)

Fig. 3.6 I_D-V_{GS} characteristics in WSe_2 FET measured by pulsed *I-V* method with (a) the t_{off} varying from 10^{-4} s to 1 s at a t_{on} of 10^{-3} s, (b) the t_{off} varying from 10^{-4} s to 1 s at a t_{on} of 10^{-4} s. The V_{base} and V_D are 0 V, and -0.1 V, respectively.

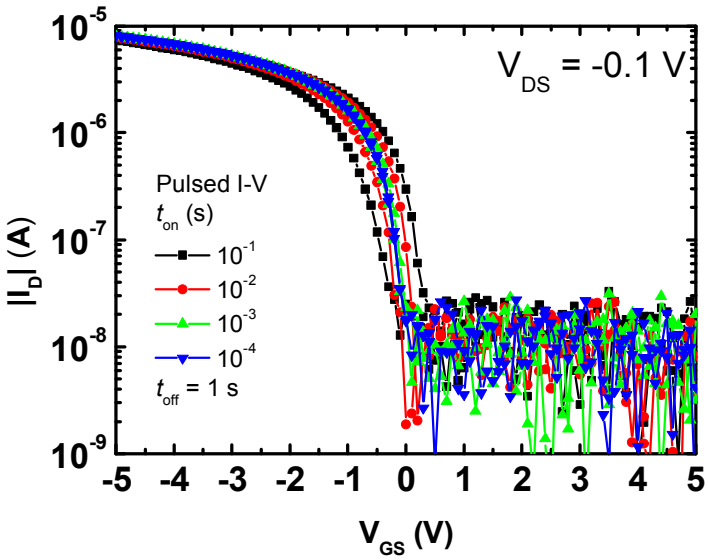


Fig. 3.7 I_D-V_{GS} characteristics in WSe_2 FET measured by pulsed *I-V* method with the t_{on} varying from 10^{-1} s to 10^{-4} s at a t_{off} of 1 s. The V_{base} and V_D are 0 V, and -0.1 V, respectively.

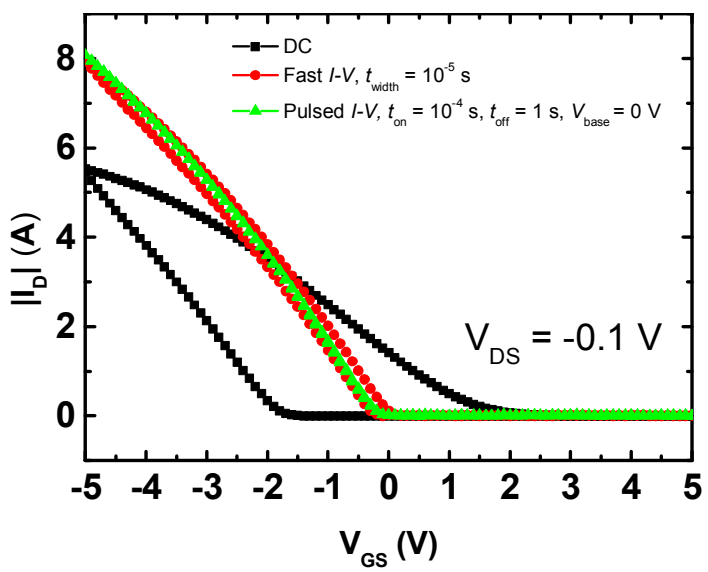


Fig. 3.8. Comparison of I_D-V_G characteristics in WSe_2 FET measured by the DC, fast *I-V* (t_{width} = 10^{-5} s), and pulsed *I-V* (t_{on} = 10^{-4} s, t_{off} = 1s, V_{base} = 0V).

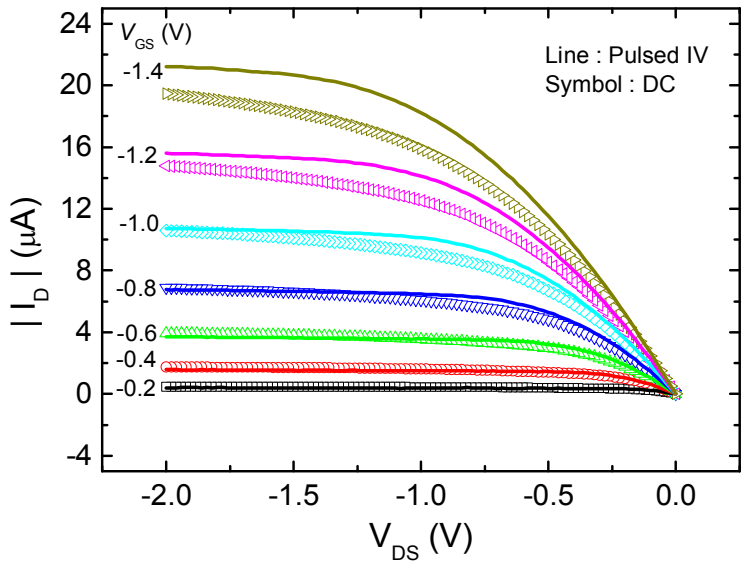


Fig. 3.9. I_D-V_{DS} characteristics in WSe_2 FET measured by pulsed I-V (t_{on} = 10^{-4} s, t_{off} = 1s, V_{base} = 0V).

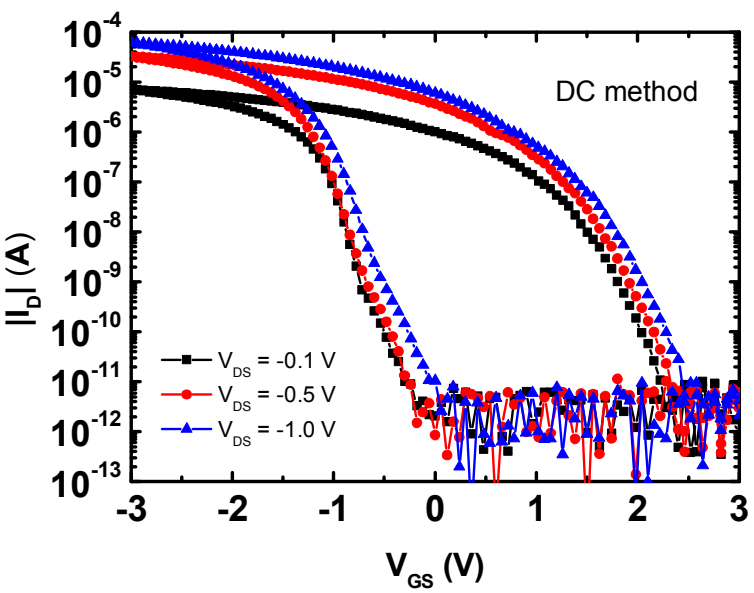


Fig. 3.10. I_D-V_{GS} characteristics in WSe_2 FET measured with various V_{DS} (-0.1, 0.5, and -1 V).

Chapter 4

Low frequency noise characteristics in WSe2 FET

4. 1 Introduction

Low-frequency noise is a significant the performance limitation of nanoscale electronic devices such as transition metal dichalcogenides (TMDCs) field effect transistors (FETs) because of a large surface-to-volume ratio [26]. Furthermore, low frequency noise characteristics should be carefully investigated because of their inherent structures of 2D van der Waals materials, which are easily prone to physical adsorption or/and chemisorption via surface contaminants on TMDCs [11, 12]. In addition, the low frequency noise analysis can further help identify sensitive areas for current transport and determine the impact of technology on device quality and reliability [27]. Nevertheless, research activities, especially for low frequency noise properties which can be one of key aspects for the “all-surface” structure of 2D materials [28, 29], have been rarely reported for WSe_2 FETs as one of promising p-type candidates in

TMDCs, whereas low frequency noise characteristics for typical n-type MoS_2 FETs have been actively researched [30-32].

4.2 Measurement scheme

Fig. 4.1 shows scheme of noise measurement system. The gate and drain voltages were kept constant during the noise measurements, where the bias voltages were supplied by using an Agilent b1500a. Low noise amplifier (LNA) converts the current fluctuation into a fluctuating voltage. Agilent 35670a dynamic signal analyzer converts dynamic signal into power spectrum density. The frequency range for low-frequency noise measurements is typically from 10 Hz to 1.6 kHz.

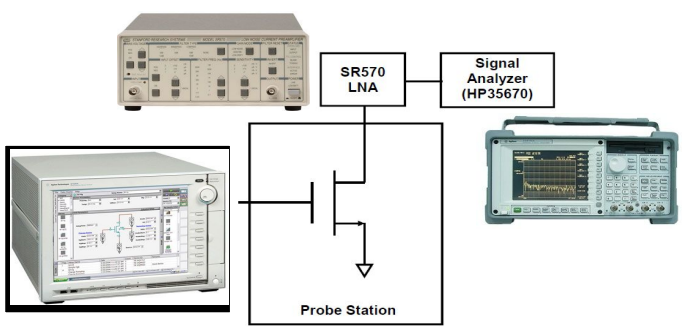


Fig. 4.1 Scheme of low frequency noise measurement system.

4.3 Measurement results

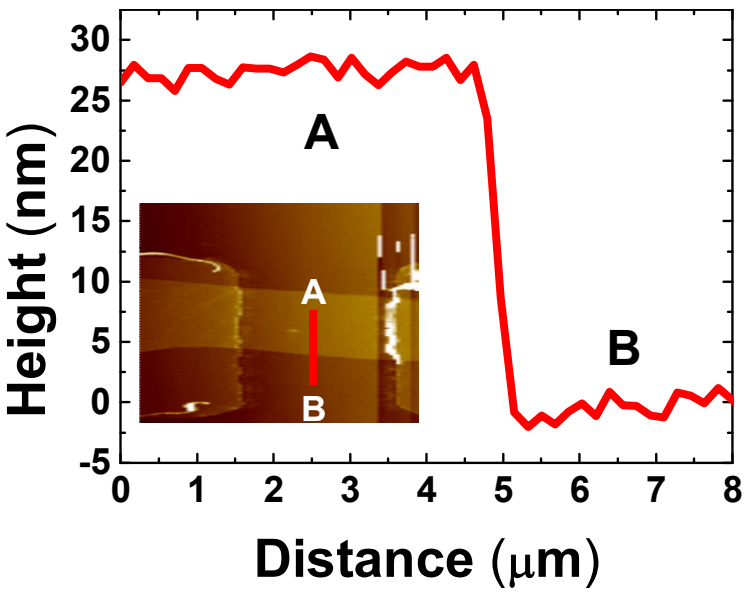


Fig. 4.2 Height profile for a multilayer in the channel of representative WSe_2 FETs. The inset shows the AFM images for the channel regime for WSe_2 FETs

Fig. 4.2 depicts height profile at the edge of the flake. The inset was AFM image of a fabricated multilayer WSe_2 FET. From AFM measurements, the thickness of the active layer used for measurement was about 28 nm in chapter 4.3.

Fig. 4.3 (a) shows the transfer characteristics of a fabricated multilayer WSe_2 FET with a ratio of width to length (W/L=15/10 μm) at a drain-to-source voltage (V_{DS}) of -0.1 V. The electrical characteristics of the devices were measured by using a precision semiconductor parameter analyzer (Agilent B1500A). The curves show typically observed p-type behaviors with a sub-threshold slope (S) of 120 mV/dec., a field effect mobility (μ_{FE}) of 80 $cm^2/V \cdot sec.$, a threshold voltage (V_{th}) of -0.7 V, and an on/off ratio of ~10^6, where V_{th} was calculated by fitting a straight line to the measured transfer curve. The field effect mobility was extracted from maximum point of transconductance (g_m). Fig. 4.3 (b) shows the output curves for the fabricated WSe_2 FET, which exhibits a clear current saturation and pinch-off behavior. In addition, current crowding around low drain bias (~-0.1V) was not observed, which indicates that good Ohmic contacts between WSe_2 and Pd were formed.

Fig. 4.4 (a) shows the S_{ID} of the device measured in the sub-threshold, linear and saturation. Measured S_{ID} nicely follows the behavior of $1/f^{\gamma}$ where the γ is close to 1 in the frequency less than ~200 Hz in all operation regimes.

Historically, two different mechanisms [33] have been considered to explain the 1/f noise in metal-oxide-semiconductors (MOS) FETs associated with fluctuations in carrier mobility (Hooge) [34] or carrier number (McWhorter) [35]. Carrier mobility fluctuation is mainly caused by lattice scattering of carrier [34], whereas carrier number fluctuation is predominately attributed to the number of carrier fluctuating due to trapping-detrapping process [35].

One of methods to distinguish the origin of fluctuations coming from carrier mobility (or carrier number) in FETs is to analyze the S_{ID} of the drain current under gate and drain bias condition. In sub-threshold and linear regime, the drain bias was fixed at -0.1 V and the gate bias was changed from -0.03 V to -1.4 V. Fig. 4.4.(b) shows that the S_{ID} versus drain current has a linear relationship from sub-threshold to linear regime, which substantiates that the low frequency noise is mainly coming from the carrier mobility fluctuation. From Hooge's empirical law, the S_{ID} can be expressed as Eq. (4.1) [36].

$$S_{ID} = \frac{q\mu_{eff}}{L^2}\frac{\alpha_H}{f} I_{DS} V_{DS} \qquad \text{Eq. (4.1)}$$

Where f is the frequency, q is the elementary electron charge, and α_H is Hooge's parameter that is subject to compare the noise level in different devices and materials. Furthermore, Fig. 4.4. (b) shows that the S_{ID}, measured in the saturation regime, is approximately proportional to the 3/2 order of I_D. The result hints that mechanism of low frequency noise in the saturation regime is also coming from carrier mobility fluctuation. In the saturation regime, Hooge's empirical relation can be expressed as Eq. (4.2) [37].

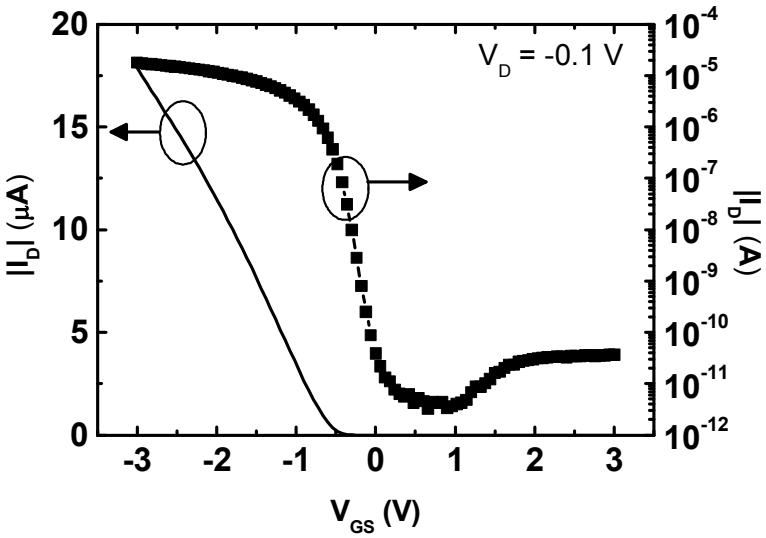
$$S_{ID} = \frac{\alpha_H}{f} q\sqrt{2}\frac{\mu_{eff}^{1/2}}{C_i^{1/2} W^{1/2} L^{3/2}} I_{DS}^{3/2} \qquad \text{Eq. (4.2)}$$

Low frequency noise characteristics for WSe_2 FETs in this study show that the behavior of flicker noise consistently obeys the Hooge's empirical laws (i.e.,

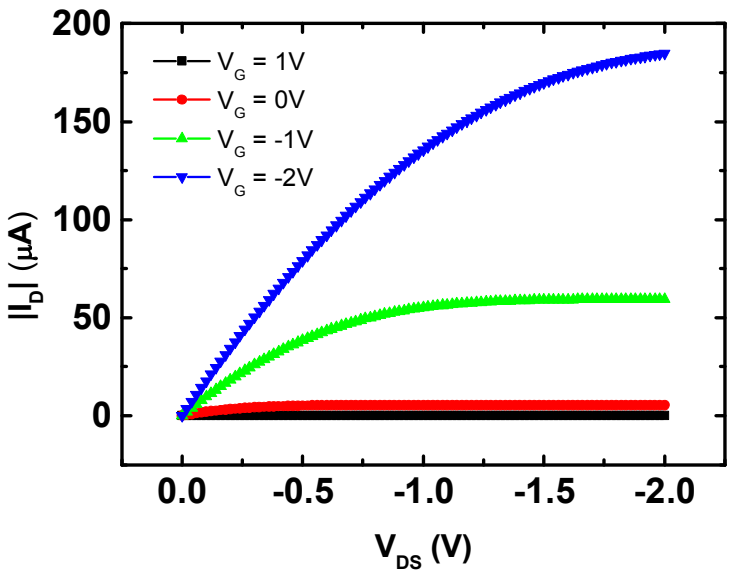
carrier mobility fluctuation) in all operation regime (linear, sub-threshold, and saturation regime). This implies that the influence of traps nearby the interface between gate dielectric (~SiO_2) and multi-layers of WSe_2 is significantly weak in the transport of the channel carriers, which might be related with the accumulated channel charge distribution deeply located from the interface [10]. The origin of the distribution is probably associated with a long Thomas-Fermi charge screening length (~7 nm), possibly observed for van der Waals layered WSe_2, which has been reported for MoS_2 FETs with multi-layers (~40 nm) [38]. In addition, encapsulation of CYTOP can lead to the reduction of chance for carrier number fluctuation possibly caused by physical or/and chemical adsorbates on the channel of WSe_2 FETs [38]. Furthermore, the potential barrier between the multi-layer WSe_2 and the gate insulator (SiO_2), probably formed by van der Waals forces, might be one of possible reasons for weak influence from interface traps [32].

Fig. 4.3 shows several Hooge's parameters for FETs with TMDC channel layers which have been reported in the literature [39, 40]. All parameters were

extracted from the linear regime. The square symbols in Fig. 4 indicate the values of Hooge's parameters for FETs with MoS_2 channel layers synthesized by chemical vapor deposition (CVD) [39]. The extracted values (for square symbols) were estimated from the low frequency noise characteristics of MoS_2 FETs measured in air ambient. Both circle and up-triangle symbols represent Hooge's parameters extracted from FETs with exfoliated MoS_2 layers and the parameters were measured either in vacuum or air [26]. The value for down-triangle in Fig. 4 was extracted from WSe_2 FET in this work. The Hooge's parameter for WSe_2 FETs in this study is about 0.12 which is similar to (or slightly larger than) those of exfoliated MoS_2 FETs (or CVD MoS_2 FETs).

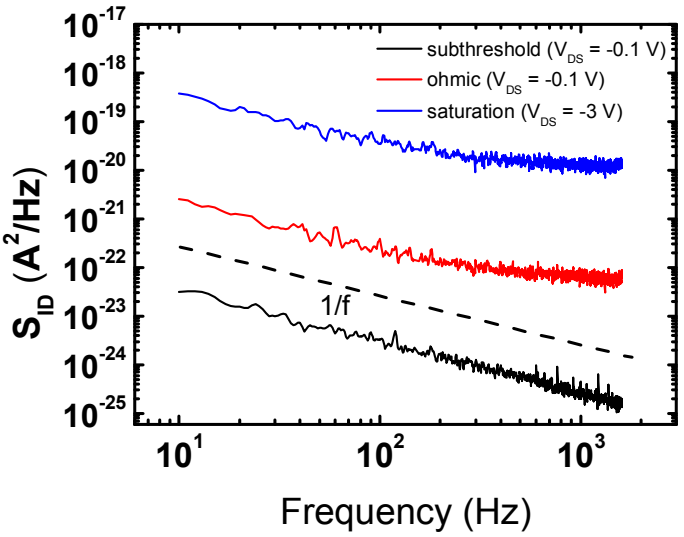


(a)

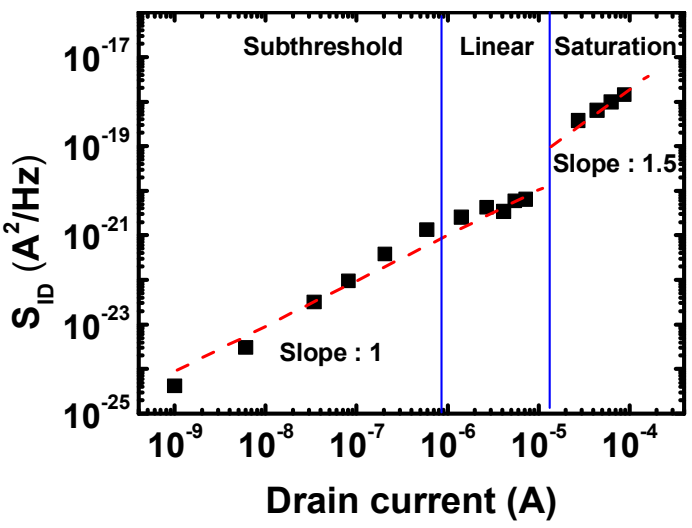


(b)

Fig. 4.3. (a) Transfer characteristics for multilayer WSe_2 FETs with CYTOP passivation measured in the linear operation regime at the drain bias of V_{DS}= -0.1V. (b) Output characteristics for the same device correspond to gate bias values from 1V to -2V, with -1V step, for the drain bias (V_{DS}) from 0V to -2V.



(a)



(b)

Fig. 4.4. (a) Drain-current noise spectral densities S_{ID}'s for the device which were measured at different operation regimes, respectively; sub-threshold (V_{GS} = -0.03 V, V_{DS} = -0.1 V), linear (V_{GS} = -0.8 V, V_{DS} = -0.1 V) and saturation regimes (V_{GS} = -1 V, V_{DS} = -3 V). (b) Measured noise power spectral densities (S_{ID}) vs drain current (I_D) at a fixed freque-ncy of 10 Hz. The bulk mobility fluctuation was observed in all operation regimes.

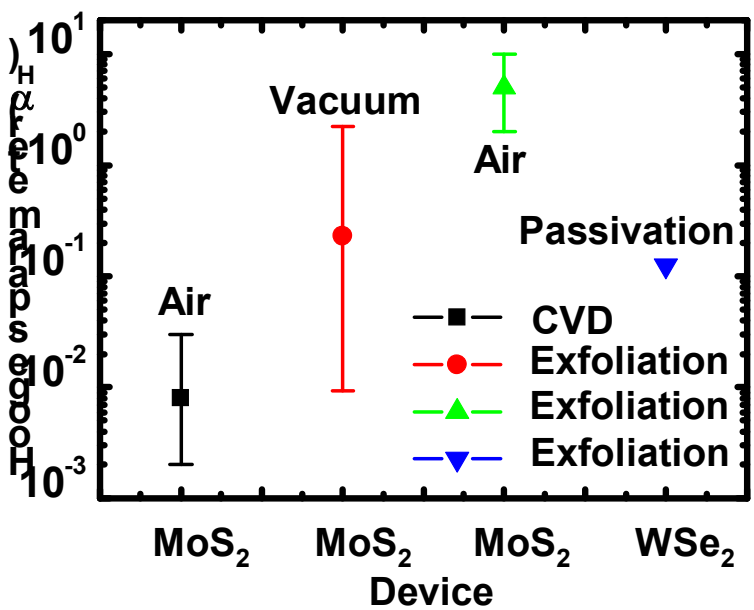


Fig. 4. 5. Extracted Hooge's parameters for MoS_2 and WSe_2 FETs which have been reported in the literatures. Each symbol for square(■), circle (●) and up-triangle (▲) corresponds to MoS_2 FETs. However, fabrication method, number of flakes and measurement environments were not exactly the same. The down-triangle(▼) indicate the data for WSe_2 FET in this experiment.

4.4 Temperature effect on low frequency noise

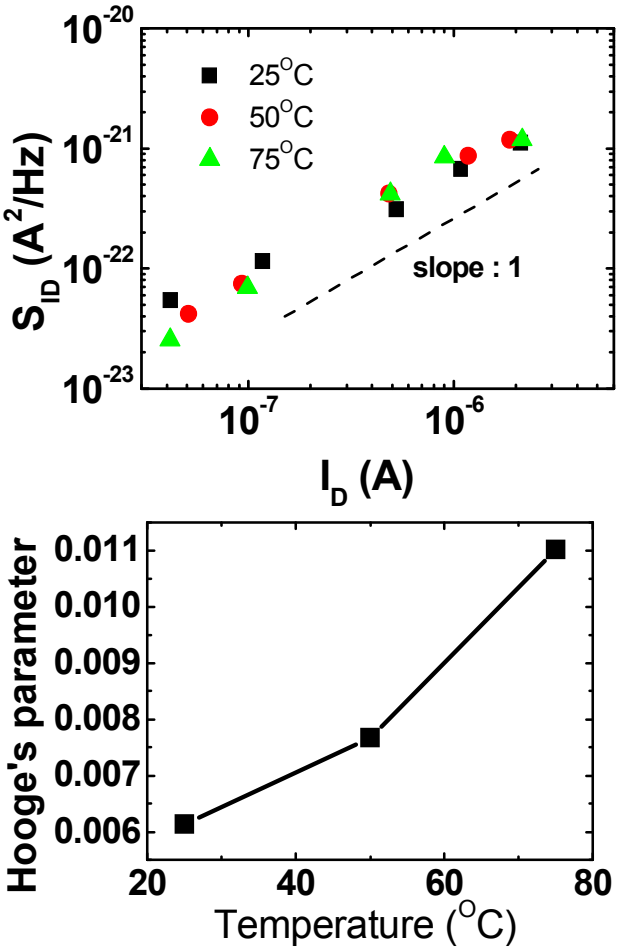


Fig. 4.6 (a) Measured noise power spectral densities (S_{ID}) vs drain current (I_D) at a fixed frequency of 10Hz and (b) extracted Hooge's parameters at different temperature.

Fig. 4(a) shows that the noise power spectral densities (S_{ID}) versus drain current has a linear relationship at various temperature (25 ^{o}C ~ 75 ^{o}C). In the Fig 4.2, the carrier mobility fluctuation is main mechanism of low frequency noise in multilayer WSe_2 FETs at room temperature. Although low frequency noise measure at different temperature, the mechanism of low frequency noise is not changed. Fig. 4(b) show the Hooge`s parameter extracted from Eq. (4.3) [36, 37].

$$S_{ID} = \frac{q\mu\alpha_H}{L^2 f} I_D V_{DS} \qquad \text{Eq. (4.3)}$$

Where f is the frequency, q is the elementary electron charge, and α_H is Hooge's parameter that is subject to compare the noise level in different devices and materials. The extracted Hooge`s parameter slightly increased with temperature increase. It is because of enhanced phonon scattering [40].

Chapter 5

CMOS inverter fabrication using a multilayer WSe_2

5. 1 Introduction

Recently, most of research activities related to WSe_2 have been noticeably toward field effect transistors (FETs) with typical *p*-type properties since WSe_2 FETs with various metals as source and drain (S/D) contact electrodes are hard to have *n*-type properties due to the metal Fermi level pinning [41] close to the particular point of the bandgap of WSe_2 [42]. For this reason, a complementary metal oxide semiconductor (CMOS) technology [43], which comprises of *p*- and *n*-type WSe_2 FETs, is a challenging technology in the absence of a controllable doping scheme [44]. Lately, gas phase doping [45] or electrostatically doping [46] has been adopted in WSe_2 FETs for the CMOS inverter. However, the WSe_2 CMOS inverter using gas phase doping has severe problems with unstable doping process in air and necessity of additional encapsulation techniques. In case of the electrostatically doped WSe_2 CMOS technology, extra elements which lead to circuit complexity are essential for the

implementation of inverter behavior. Hence, another way to achieve WSe_2 CMOS technology is needed to design integrated circuits (IC). In this chapter, author demonstrate reasonable *p*- and *n*-type characteristics of multi-layer WSe_2 FETs fabricated on the same substrate, and show reasonable *I-V* characteristics without extra doping scheme.

5. 2 Fabrication process of CMOS inverter

Fig. 5.1 (a) shows cross-sectional schematic view of a fabricated CMOS inverter based on multi-layer WSe_2 FETs on the same substrate. An *n*-type Si wafer with a heavy phosphorus doping (ρ~0.005 ohm·cm) is used as a starting substrate, which plays a role as back-gate electrode in WSe_2 FETs. Through a thermal oxidation in dry oxygen at 950 °C, 35 nm thick thermal SiO_2 waa grown on the heavily doped Si wafer and served as a gate insulator. A lift-off process was performed to form alignment marks on each sample. A layer of photoresist (PR) was coated and patterned, and then ~50 nm thick Cr deposition was followed by the removal of the PR. The multi-

layer WSe_2 flakes were mechanically exfoliated from bulk WSe_2 crystals by using PDMS stamp and transferred onto the SiO_2 layer formed on the Si substrate. The WSe_2 flakes on the substrate were annealed at 350 ºC for 2 hours in the ambient of a mixed gas of argon and hydrogen for reducing interface traps. PR patterning with a length (L) of 10 μm for both *p*- and *n*-type FETs was followed by UV treatment at a wavelength of 185 nm for 5 min to remove residues that may come from the transfer of flakes and patterning process. Then a layer of metal was deposited to provide the S/D electrodes. Au and Al films with a thickness of ~100 nm were formed by electron beam evaporation for the source/drain electrodes of *p*- and *n*-type FETs, respectively. The PR was removed in acetone. After forming S/D electrodes, the thickness of WSe_2 flakes for both *p*- and *n*-type FETs was measured by using atomic force microscopy (AFM) as shown in Fig. 5.1 (b) and (c). The thicknesses of multi-layer WSe_2 flakes for both *p*- and *n*-type FETs were about 38 nm which approximately corresponds to 55 layers. Note approximate channel width was ~30 μm. For preventing the devices from

being degraded in performance by permeation of moisture, the backside of WSe_2 flakes was encapsulated by fluorinated polymer (CYTOP; CTL-809M, Asahi Glass Co. Ltd) with a spin coating process. The CYTOP as a hydrophobic polymer allows multi-layer WSe_2 FETs to operate stably in air. Finally, pad opening is conducted. Since the PR cannot be coated on the CYTOP having a hydrophobic characteristic, ~50 nm thick SiO_x was formed on the CYTOP by thermal evaporation. Then PR was coated, and patterned by using the mask for the pad open. The SiO_x and CYTOP were removed sequentially by dry etching in a gas ambient of ~O_2/CF_4. The electrical characteristics of devices and inverter were measured at room temperature by using a precision semiconductor parameter analyzer (Agilent B1500A).

Fig. 5.2 (a) and (c) display the drain current (I_D) versus gate bias (V_{GS}) curves measured from the fabricated *n*- and *p*-type multi-layer WSe_2 FETs at a drain voltage (V_{DS}) of 1 V and -1 V, respectively. In WSe_2 FET having Al as the S/D electrodes, the curves show *n*-type behaviors with an on-current density of 0.13 μA/μm at V_{DS} = 1 V, a *SS* of 310 mV/decade, an on/off ratio

of 10^6, and a threshold voltage (V_{th}) of 1.8 V. In *p*-type WSe_2 FET, Au is used as the S/D electrodes. The I_D-V_{GS} curves show typically *p*-type behaviors with an on-current density of 0.46 μA/μm at V_{DS} = -1 V, a *SS* of 220 mV/decade, an on/off ratio of 10^6, and a V_{th} of -1.4 V. The V_{th} is calculated by fitting a straight line to the linearly increasing I_D and extrapolating the line to an intercept on the *x*-axis. Fig. 5.2 (b) and (d) show output characteristics (I_D-V_{DS}) of *n*- and *p*-type multi-layer WSe_2 FETs, respectively. The *n*-type FET has a higher saturation voltage than *p*-type due to a higher contact resistance between the Al and the WSe_2. The higher contact resistance effect is clearly observed in linear I_D-V_{GS} curve in Fig. 5.2 (a) where the I_D starts to saturate at a V_{GS} of ~3 V. Moreover, the electron mobility extracted from linear I_D-V_{GS} curve of *n*-type FET in Fig. 5.2(a) is actually three times lower than that from linear I_D-V_{GS} curve *p*-type FET in Fig. 5.2(c).

The type of a FET is determined by the polarity of carriers (electrons or holes) that are injected from the source contact. In FETs with a Schottky

barrier in the source and drain regions, the polarity and the injection efficiency of the carriers are determined, respectively, by the work-function difference and the Schottky barrier height at the contact between the semiconductor and the metal electrode [47]. Therefore, the selection of the S/D electrodes to control the Schottky barrier property is a crucial point of device design since there is lack of a substitutional doping scheme in low dimensional system.

In fact, it has been reported that WSe_2 FETs have typically *p*-type conducting behaviors by adopting Pd as a high work-function metal for the S/D electrodes in recent works [11]. This indicates that the Fermi level of the Pd aligns close to the valence band of WSe_2, and hole injection is more efficient thanks to relatively low Schottky barrier for holes. This property of WSe_2 indicates that the fabrication of complementary logic circuits is possible if high performance *n*-type WSe_2 FETs can be achieved by selecting a proper metal as the S/D contact electrode.

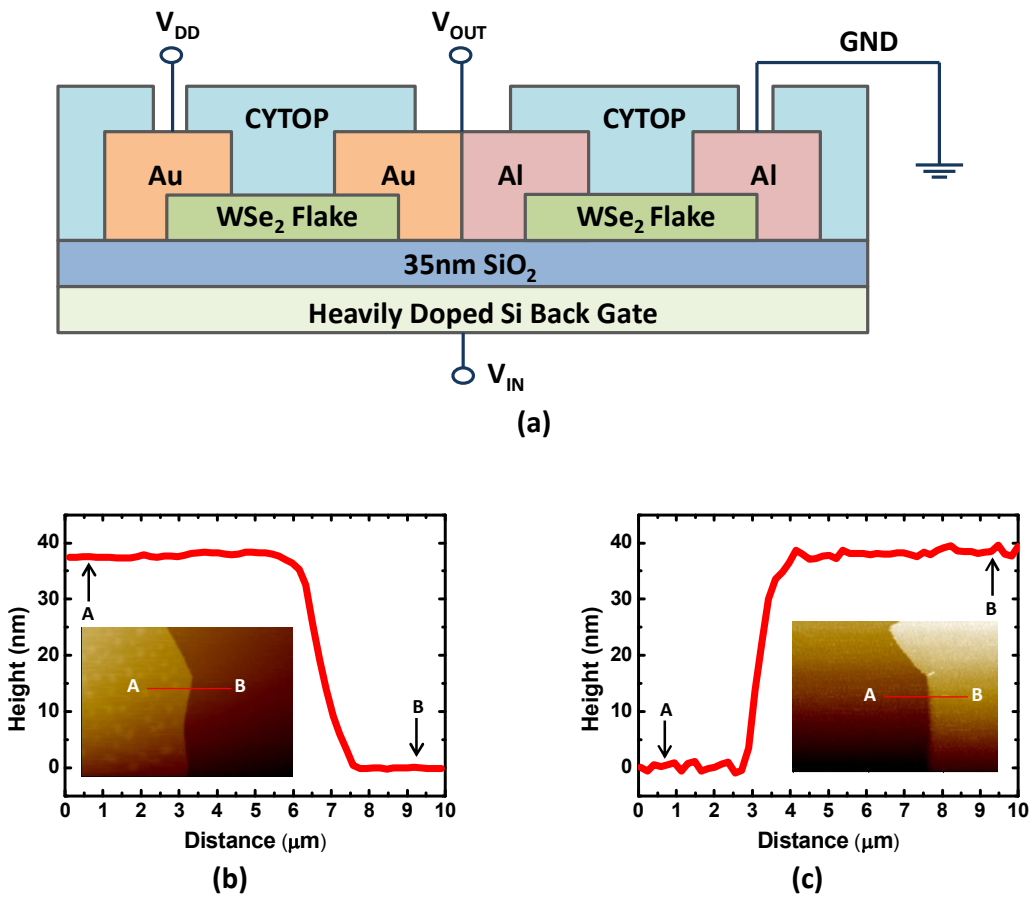


Fig. 5.1. (a) A cross-sectional schematic view of a CMOS logic inverter composed of multi-layer WSe_2 FETs. The thickness of multi-layer WSe_2 flakes for a *p*-type (b) and an *n*-type (c) FETs is ~38 nm, which corresponds to 55 layers. The thickness was obtained by scanning the tip of atomic force microscope along the red line from A to B. The insets in Fig. 5.1 (b) and (c) show the AFM images for the multi-layer WSe_2 flakes.

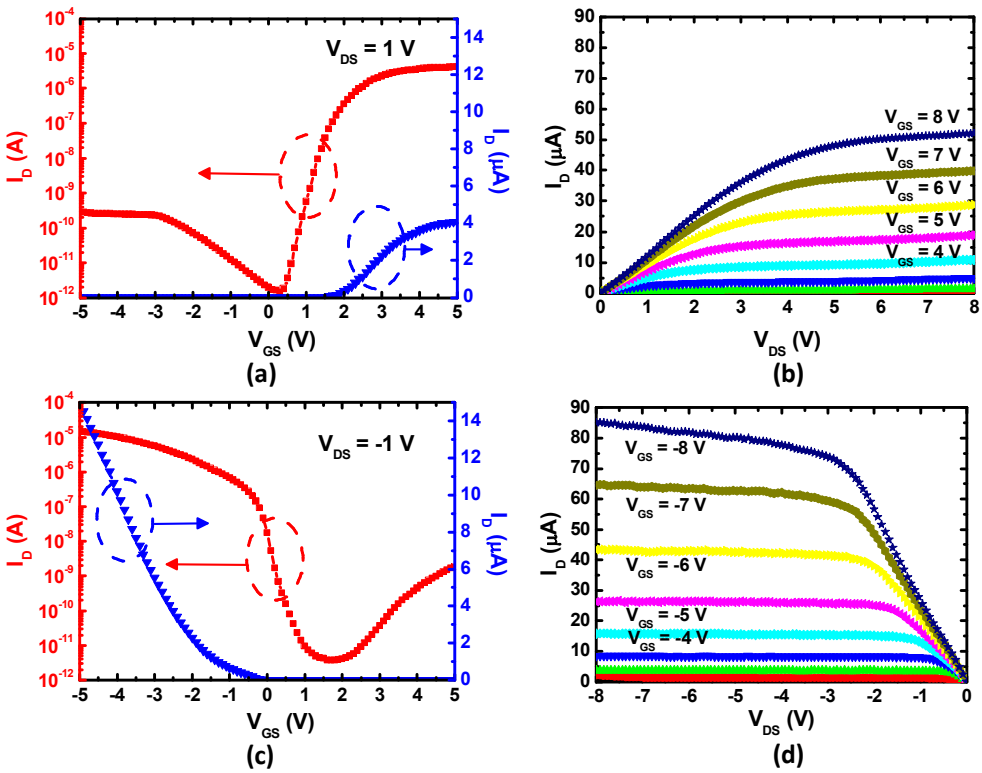


Fig. 5.2. Transfer (I_D-V_{GS}) characteristics measured from (a) *n*- and (c) *p*-type multi-layer WSe_2 FETs with CYTOP passivation at a drain bias (V_{DS}) of 1 V and -1 V, respectively. Figures (b) and (d) show output (I_D-V_{DS}) characteristics measured from *n*- and *p*-type multi-layer WSe_2 FETs as a parameter of V_{GS}, respectively.

Fig. 5.3 shows the work-functions of several candidates for the S/D metal electrodes, and energy band diagram of a multi-layer WSe_2. To achieve a high-performance CMOS logic inverter, high and low work-function metals are needed for efficient injection of holes and electrons in *p*- and *n*-type WSe_2 FETs, respectively. Theoretically, a low work-function metal is desirable to achieve a small electron Schottky barrier height with WSe_2 for *n*-type FET. Hence, Ag, Al and Mg are potential candidates as the S/D electrode for *n*-type WSe_2 FET. Among three candidates, Mg is the best S/D electrode on WSe_2 to give a good Ohmic-like contact since Mg has the smallest work-function. However, Mg is not suitable for contact electrode because of its high reactivity with oxygen in air. As the second candidate, Al with a work-function close to the electron affinity of WSe_2 would also lead to a small Schottky barrier for electrons, thereby resulting in a high-performance *n*-type FET. As expected, the WSe_2 FET with Al electrodes as the S/D metal has *n*-channel transistor behavior. However, the on-state performance of an *n*-type WSe_2 FET is limited since the metal Fermi level is pinned close to the middle of the band gap of WSe_2 [49]. To reduce the on-

current difference between *p*- and *n*-type FETs at the same *L* and similar channel width, Au as the S/D electrodes for *p*-type FET is selected in this work although the work-function of Pd is higher than that of Au.

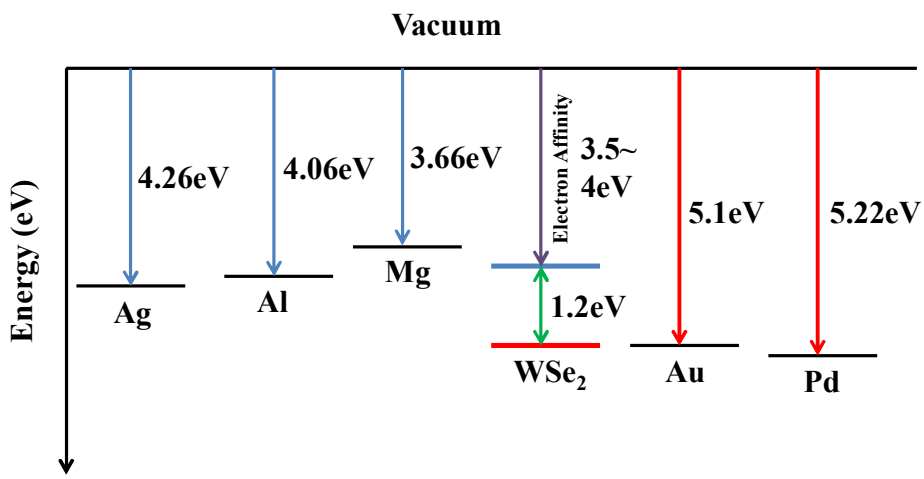


Fig. 5.3. Band alignments of some potential S/D metals with respect to the energy band of the multi-layer WSe_2.

5. 3 Measurement results

The *p*- and *n*-type WSe_2 FETs described above are connected in series to compose a CMOS logic inverter. A supply voltage (V_{DD}) is applied to the source of the *p*-type FET and the source of the *n*-type FET is grounded. The n^+ substrate (back-gate) is used as the input terminal, and the Au and Al electrodes for the drain of both FETs are used as the output terminal of the inverter.

The corresponding voltage transfer characteristics (VTC) of the fabricated CMOS logic inverter are shown in Fig. 5.4 as a parameter of V_{DD} from 2 V to 8 V. The VTC displays excellent inverting performance with a full logic swing, abrupt transition, and almost zero current under static condition. For a low V_{DD} (for example, 2 V), the logic transition occurs at a V_{IN} close to V_{DD}, since the *p*-type FET has relatively higher I_D than the *n*-type FET at a lower V_{GS} due to lower V_{th} and higher mobility.

Fig. 5.5 (a) shows the voltage gain of the CMOS logic inverter consisted of two multi-layer WSe_2 FETs. The maximum of the voltage gain, which is defined as $-dV_{OUT}/dV_{IN}$, represents the sharpness in transition region between two logic

states. The transition region widths, which can be defined as the region where the gain is larger than 1, under different V_{DD}s are plotted in Fig. 5.5 (b). The voltage gains of the fabricated CMOS logic inverter are higher than 25 for given V_{DD}s from 2 V to 8 V. Moreover, the transition regions for all V_{DD}s are less than 0.35 V. Although the current drivability of both *p*- and *n*-type FETs in an inverter is not optimized in this work, the gain of the inverter is relatively high.

Noise margin is another important factor for determining sensitivity and tolerance with respect to signal interference in logic gates. Noise margin can be calculated by extracting ideal logic-high voltage V_{OH}, ideal logic-low voltage V_{OL}, maximum low input voltage in transition region V_{IL}, and minimum high input voltage in transition region V_{IH}. Therefore, noise margins for logic state 1 (NM_H) and logic state 0 (NM_L) are defined as $NM_H=V_{OH}-V_{IH}$ and $NM_L=V_{IL}-V_{OL}$. In this work, the normalized total noise margins to V_{DD}, which can be defined as $(NM_L+NM_H)/V_{DD}$, measured at different V_{DD}s are higher than ~0.9, which is close to 1 (ideal), as shown in Fig. 5.5 (b).

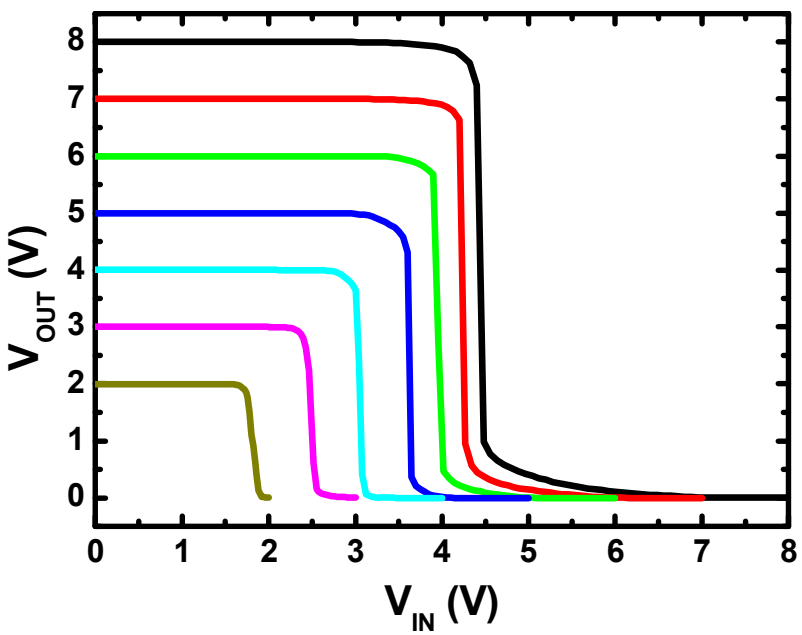
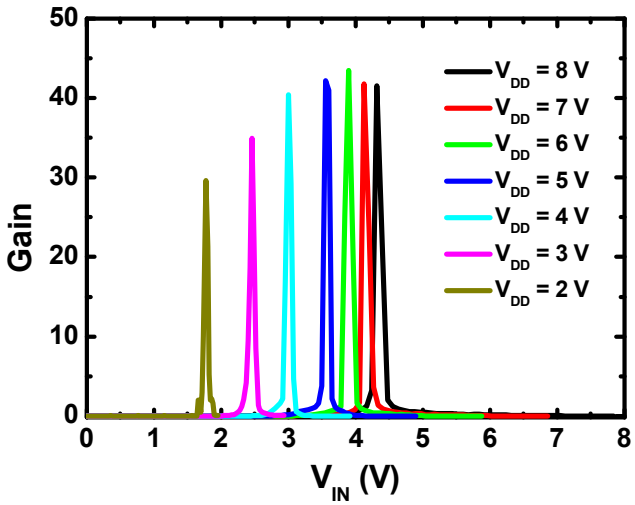
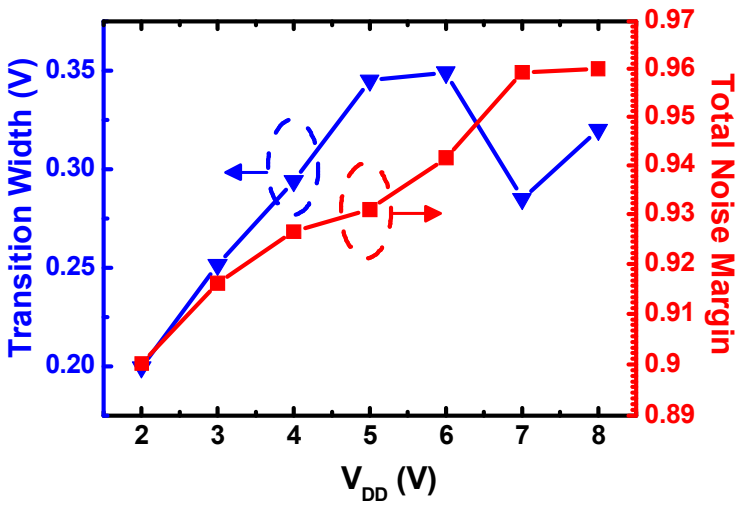


Fig. 5.4. Voltage transfer characteristics (output voltage as a function of the input voltage) of a CMOS logic inverter consisted of *p*- and *n*-type multi-layer WSe_2 FETs as a parameter of V_{DD} from 2 V to 8 V.



(a)



(b)

Fig. 5.5. (a) Voltage gain of a CMOS logic inverter composed of *p*- and *n*-type multi-layer WSe_2 FETs. The peak voltage gains for given V_{DD}s from 2 V to 8 V are larger than 25. The V_{IN}s corresponding to the peak gains are logic transition voltages for given V_{DD}s. (b) Transition width and the normalized total noise margin to V_{DD} are shown on the left and right *y*-axes, respectively, as a function of V_{DD}.

Chapter 6

Contact property improvement using a hole injection layer

6. Introduction

Above mentioned in chapter 1. TMDC have been investigated as candidate materials for next generation nano electronic devices with their outstanding electrical properties. Among various TMDCs FET, especially WSe_2 FET, has drawn attention to the possibility for its applications of nanoscale complementary circuits and switching back planes for high resolution flat panel display (FPD) due to their high mobility (~100 $cm^2/V \cdot s$), excellent on/off ratio (~10^7), and low subthreshold slope (*SS*, ~ 70 mV/decade). However, lack of doping process is critical issue for high performance WSe_2 FET, because of high contact resistance. A high contact resistance has been found to be a key factor that can significantly influence device performance of multilayer WSe_2 FETs

[15]. In addition, Fermi level pinning effect induce the undesirable Schottky contact between WSe_2 flake and metal. Fig 6.1 shows the *I-V* characteristic of Au-WSe_2-Pd vertical structure. In Fig 6.1, Schottky diode characteristics was clearly shown in spite of using a high work function metal (Au). It is because of Schottky contact between of WSe_2 flake and Au. Figure 6.2 shows effective barrier height versus contact metal work function. Here, S parameter (pinning factor) close to zero [50]. It represent the fermi level pinning occur WSe_2 flake. Lately, gas phase doping [11] or Ohmic contact for high work function metal [15] has been adopted in WSe_2 FETs low contact resistance. However, gas phase doping has severe problems with unstable doping process in air and necessity of additional encapsulation techniques. And high work function metal like a Pd is bad cost effect for commercialization. In this chapter, contact property improve and reduce the Schottky barrier height using an oxygen plasm treatment.

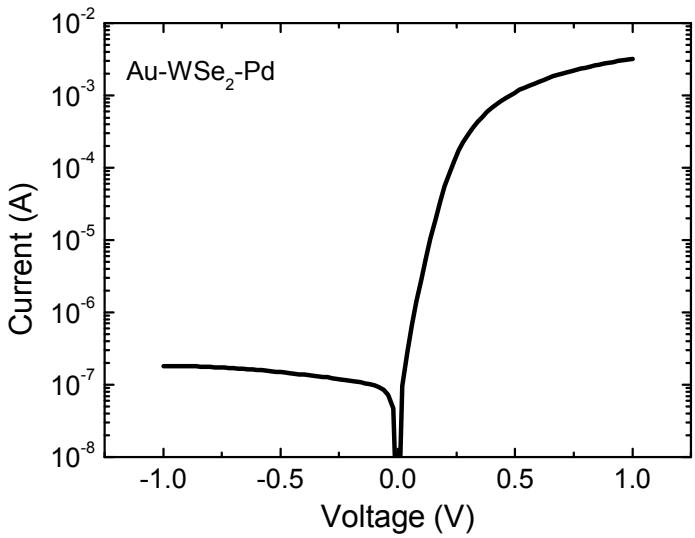


Fig. 6.1 *I-V* characteristic of Pd-WSe_2-Pd vertical structure.

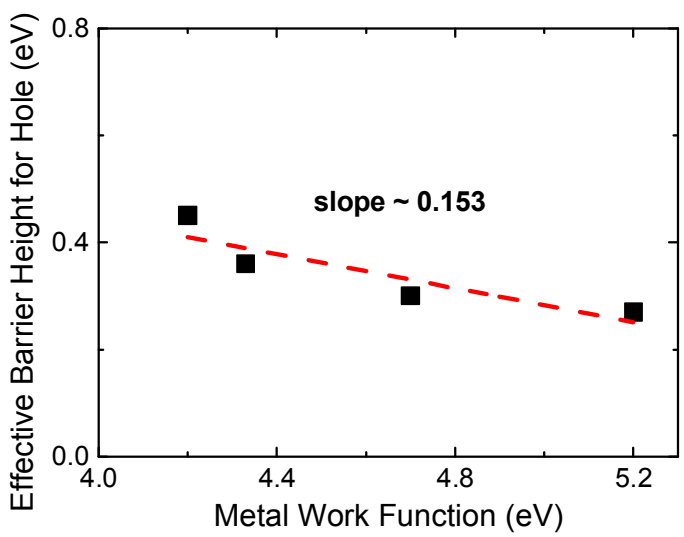


Fig. 6.2 Extracted effective barrier height for holes as a function of metal work function.

6. 2 Experimental detail

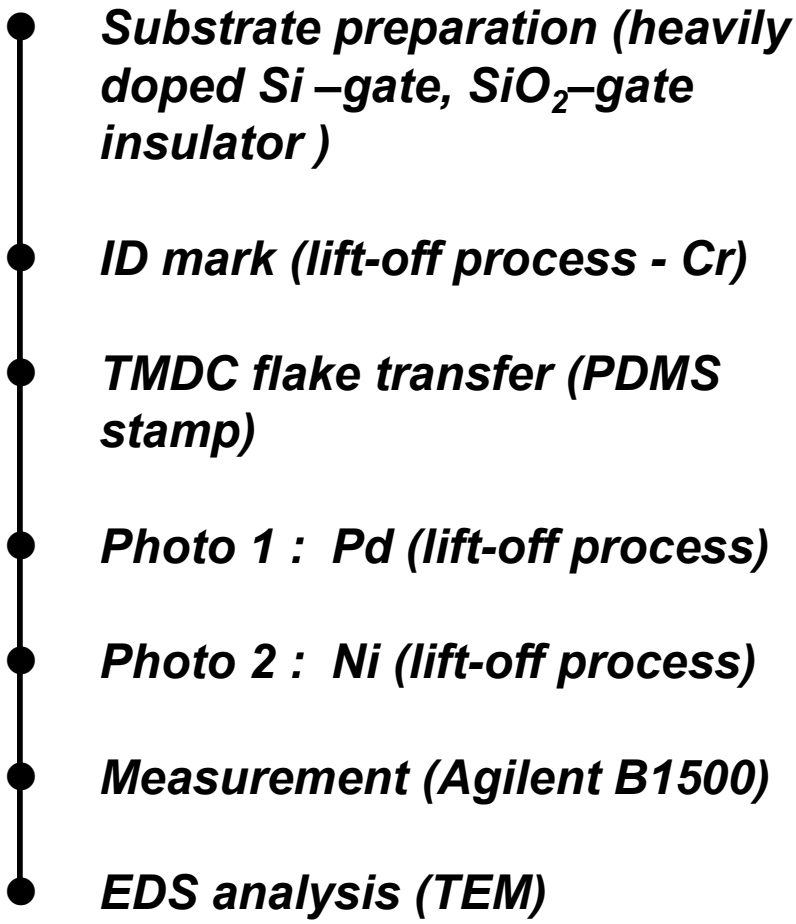


Fig. 6.3 Fabrication process flow of WSe_2 FET with different source/drain metal without oxygen plasma treatment.

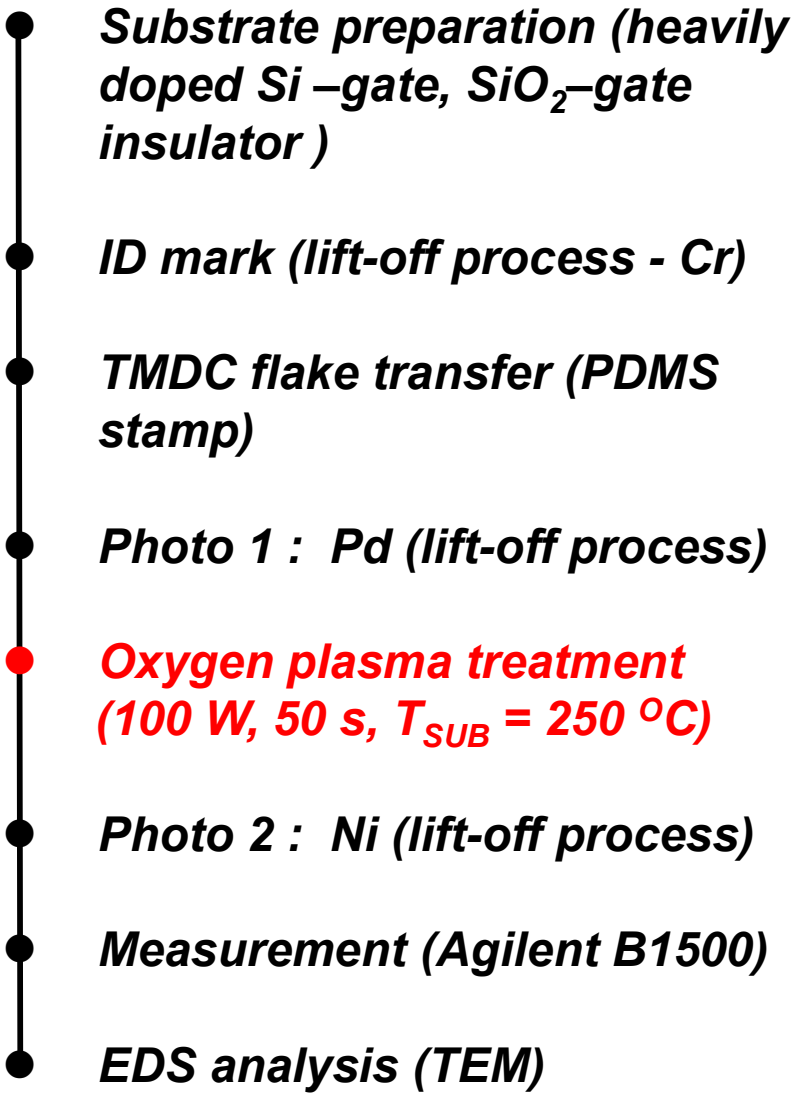


Fig. 6.4 Fabrication process flow of WSe_2 FET with different source/drain metal with oxygen plasma treatment.

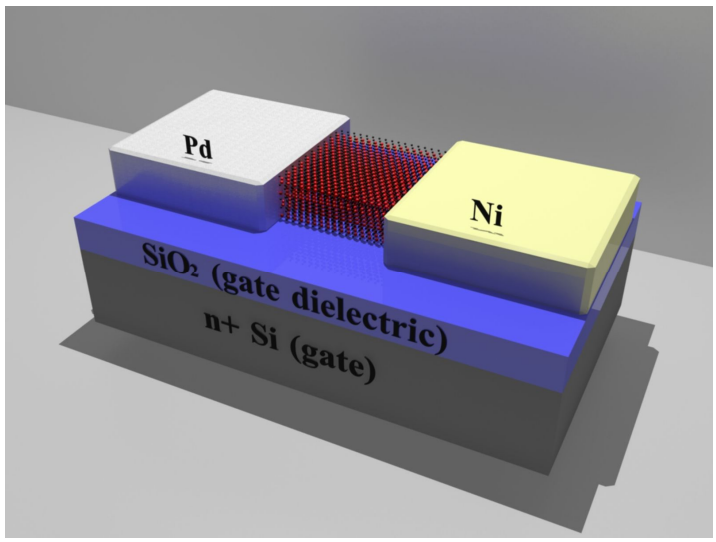


Fig. 6.5 Schematic image of a multilayer WSe_2 FET with different source/drain metal.

Fig. 6.3 and 4 show the fabrication process flow of WSe_2 FET with different source/drain metal with or without oxygen plasma treatment. Fig. 6.5 shows schematic view of a fabricated WSe_2 FET based on multi-layer WSe_2 FETs with different S/D metal. An *n*-type Si wafer with a heavy phosphorus doping (ρ~0.005 ohm·cm) was used as a starting substrate, which plays a role as back-gate electrode in WSe_2 FETs. Through a thermal oxidation in dry oxygen at 950 °C, 35 nm thick thermal SiO_2 was grown on the heavily doped Si wafer and served as a gate insulator. A lift-off process was performed to form alignment

marks on each sample. A layer of photoresist (PR) was coated and patterned, and then ~50 nm thick Cr deposition is followed by the removal of the PR. The multi-layer WSe_2 flakes were mechanically exfoliated from bulk WSe_2 crystals by using PDMS stamp and transferred onto the SiO_2 layer formed on the Si substrate. Then a layer of metal was deposited to provide the one side electrodes. Pd films with a thickness of ~100 nm were formed by electron beam evaporation. And then oxygen plasma exposure to WSe_2 flake surface. The flow rate was 50 standard cubic cm per min (sccm), the pressure was 1.3 Torr, treatment time was 50 s, substrate temperature was 250 ^{o}C, and the power was 100 W. After treatment, Ni films with a thickness of ~100 nm were formed by electron beam evaporation for the other side electrode.

6. 3 Measurement result

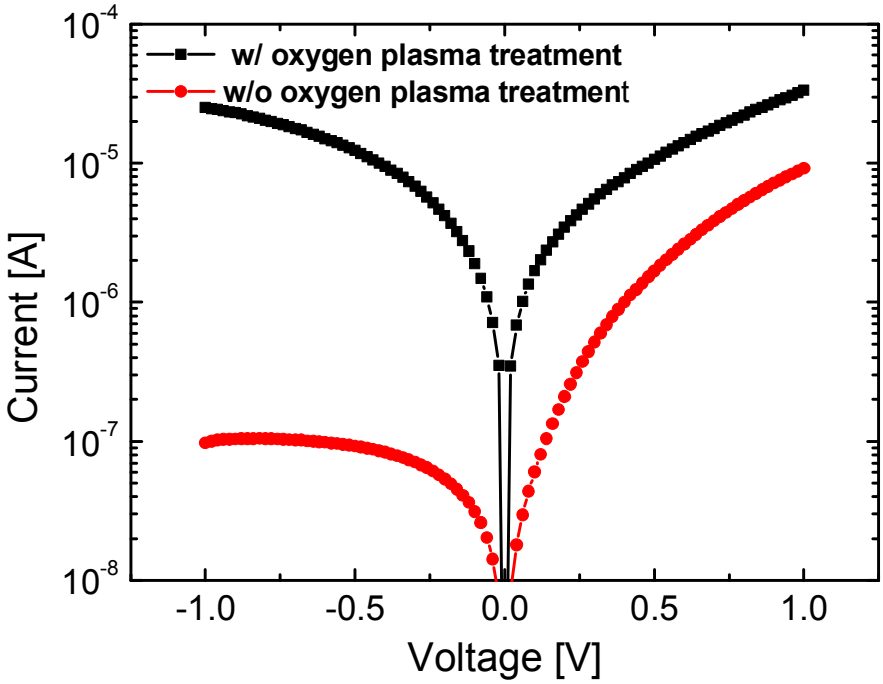
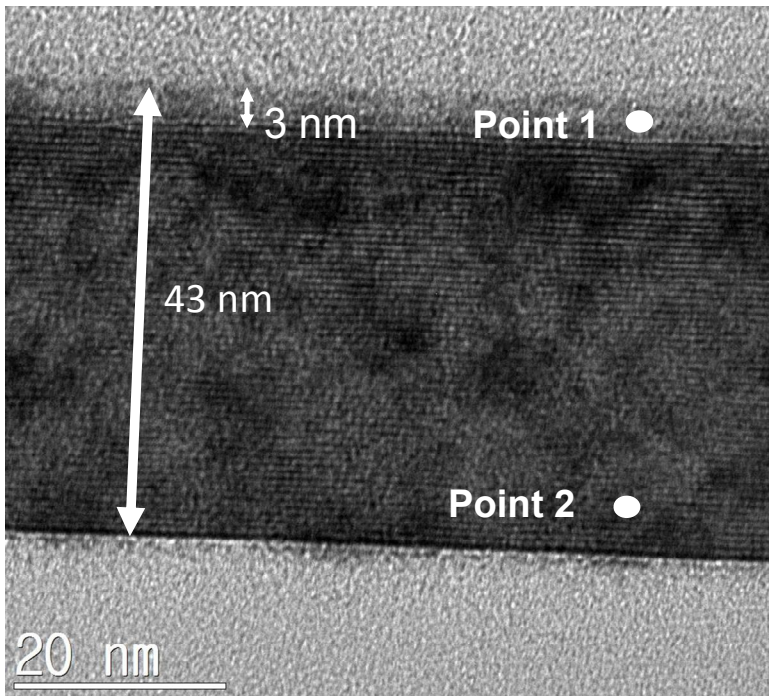


Fig. 6.6 *I-V* curves of the Pd-WSe_2-Ni lateral structure with or without oxygen plasma treatment.

Fig. 6.6 shows electrical property of WSe_2 FET with different source/drain metal with or without oxygen plasma treatment. Without oxygen plasma treatment device (●) shows Schottky diode characteristic. Here Pd was anode

electrode and Ni was cathode electrode. Though the Ni was high work function metal, Schottky contact was formed between Ni and WSe_2 due to Fermi level pinning effect. In contrast, With oxygen plasma treatment device (■) shows Ohmic behavior clearly. For the analysis of oxygen plasma treatment, transmission electron microscopy (TEM) and Energy-dispersive X-ray spectroscopy (EDS) were conducted. Fig 6.7 show the TEM image and atomic ratio of two points (surface and bulk) at WSe_2 flake after oxygen plasma treatment. In atomic ratio of point2 (bulk), flake might be deduced that it is formed of a WSe_2. However, after plasma treatment, oxygen rich flake observed. It represent that WO_3 was formed during the plasma treatment [51, 52]. WO_3 is a well-known transition metal oxide, which should exhibit a higher work function (6.4 eV) [53] and is more favorable for hole injections into the semiconductor [54].



(a)

Element	Atomic %	
	Point1	Point2
O	73.94	
Se	7.77	61.17
W	18.29	38.83
Total:	100.00	100.00

(b)

Fig. 6.7 *I-V* curves of the Pd-WSe_2-Ni lateral structure with or without oxygen plasma treatment.

Chapter 7

Conclusion

In this thesis, high performance TMDC field effect transistors (FETs) were fabricated by photo-lithography process using a mechanically exfoliated multi-layer WSe_2. Fabricated device showed a good Ohmic contact behavior and stable operation in air by adopting hydrogen annealing and hydrophobic CYTOP layer as an encapsulation layer.

In chapter3, *I-V* characteristics of WSe_2 FETs obtained by applying the DC, fast *I-V*, and pulsed *I-V* measurement methods have been systematically investigated. In the DC measurement result, large hysteresis is observed due to the V_G stress during the measurement. In the results of the fast *I-V* measurement, the hysteresis is reduced as the measuring time is shorter with a faster sweeping rate (t_{width}), however, the hysteresis is still not negligible even at the shortest t_{width} (10^{-5} s). In the pulsed *I-V* measurement, less hysteresis and enhanced mobility and conductance are obtained with increasing t_{off} and decreasing t_{on} due to reduced V_G

stress during ton and increased charge relaxation time with t_{off}. With a V_{base} of 0 V, and a short t_{on} (10^{-4} s) and a long t_{off} (1 s) of the V_G pulse in the pulsed *I-V* measurement, the hysteresis-free I_D-V_{GS} curves obtain with the noticeably enhanced mobility in WSe_2 FETs. Among three measurement methods, pulsed *I-V* measurement method provide the best performance of the device.

In chapter 4, low frequency noise characteristics of a FET with multi-layer (~27 nm) WSe_2 as a channel material was investigated at all operation regimes and various temperature. In all operation regime, the low frequency noise characteristics of the WSe_2 FET obey consistently Hooge's empirical relation, which indicates mobility fluctuation is a dominant mechanism responsible for the drain current fluctuation. These results might be attributed to weak interaction between the accumulated holes in the channel and the traps at the interface since the channel carriers in the WSe_2 are away from the interface. Extracted Hooge's parameter in this work is within the value comparable to those of the TMDC FETs in recently published literatures. Although LFN measure at different temperature, the mechanism of LFN is not changed. However, Hooge`s parameter slightly

increased with temperature increase due to phonon scattering enhancement.

In Chapter 5, CMOS logic inverter composed of multi-layer WSe_2 FETs has been demonstrated. The proposed device can be fabricated on a single substrate and have no an additional doping process. Au and Al electrodes were contacted to the multi-layer WSe_2 for p- and n-type FETs, respectively. Both FETs have shown reasonable *I-V* characteristics. Excellent inverting performance including full logic swing, high voltage gain, abrupt transition, high noise margin in the VDD range from 2 V to 8 V, was observed in fabricated logic inverter at room temperature. These results indicate that the logic inverter has a high potential for post silicon nanoelectronics. Furthermore, since two-dimensional semiconductors have many advantages in flexible applications, this work can pave the way for extending the range of application for TMDCs to flexible electronics.

Lastly, chapter 6 represents contact property improvement using an oxygen plasma treatment method. After plasma treatment, WO_3 was formed at WSe_2 flake surface. WO_3 plays a role as hole injection layer between Ni and WSe_2 flake. Contact resistance and undesirable Schottky barrier height reduced dramatically

using oxygen plasma treatment process. This has the advantage of being easy to process and method do not need an additional deposition process.

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초 록

최근, TMDC는 그들의 뛰어난 전기, 광학, 열적, 기계적 특성 때문에 차세대 나노 전자 소자 물질로 연구되고 있다. 특히 WSe_2 전계 효과 트랜지스터는 뛰어난 이동도 (~100cm^2/V·s) 와 on/off 전류비 (~10^7) 그리고 낮은 역치하 기울기 (*SS*, ~ 70 mV/decade) 를 가지기 때문에 나노 스케일의 상보형 회로와 고해상도의 평판 디스플레이의 스위칭 소자로서의 응용 가능성이 높다.

이 논문에서는 기계적으로 박리된 다층의 WSe_2를 이용 하여 고성능의 TMDC 전계 효과 트랜지스터를 제작 하였다. 제작된 소자의 DC 측정에서는 측정 중 발생하는 게이트 전압 때문에 큰 히스테리시스 차이를 보이지만 펄스를 이용한 측정에서는 히스테리시스가 거의 없고 DC측정에 비해 큰 전도도를 보이는 소자 본연의 특성을 얻을 수 있었다. 수소 열처리와 소수성의 CYTOP 층을 보호 층으로 사용 하여 히스테리시스 차이를 줄이고 전기적 특성을 크게 개선하였다. 저주파 잡음 측정으로 통해 다층의 WSe_2 전계효과 트랜지스터의 저주파 잡음 특성은 Hooge 경험식을 잘 따르며, 이는 저주파 잡음의 주요 원인이 전송자의 이동도 흔들림임을 알 수 있다. 여러 온도에서의 저주파 잡음 측정에도 불구하고, 저주파 잡음 특성은 전송자의 이동도 흔들림이 주요 원인이었고, 온도가 증가함에 따라 phonon 산란이 증가 하여 Hooge 상수도 증가함을 알 수 있다. 이러한 저주파 잡음 특성의 결과들은 Thomas-Fermi charge screening과 inter-layer resistance coupling을 뒷받침 해 줄 수 있는 자료이다. n/p 형의 WSe_2 전계 효과 트랜지스터를

이용해, 고성능의 상보형 금속 산화물 인버터를 제작하였다. p형 전계 효과 트랜지스터는 큰 일함수를 갖는 금속을 소스/드레인으로 사용 하였고, n형의 전계효과 트랜지스터는 낮은 일함수를 갖는 금속을 소스/드레인으로 사용 하여 만들어 졌다. 제작된 소자는 비슷한 on 전류 밀도와 on/off 전류비를 갖는다. 제안된 인버터는 높은 전압 이득과 높은 잡음 여유를 포함한 우수한 스위칭 특성을 보인다. 이러한 인버터 특성은 추가적인 도핑 과정 없이도 상보형 금속 산화물 회로 구현이 가능 하다는 것을 보여 준다. 마지막으로 산소 플라즈마 처리를 통해 WSe_2 계면을 WO_3 로 형성하여 전공 주입층으로 활용할 수 있는 연구를 진행하였다. 그 결과 접촉 저항이 매우 낮아졌고 원하지 않는 샤키 장벽을 없앨 수 있었다. 이러한 연구는 쉽게 전공 주입층을 형성하여 금속과 반도체 물질 사이의 접촉 특성을 개선하는데 일조 할 수 있다.

주요어 : TMDC, 전계 효과 트랜지스터, Pulsed I-V, 상보형 금속 산화물 인버터, 저주파 잡음
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